



basic education

Department:
Basic Education
REPUBLIC OF SOUTH AFRICA

ELECTRICAL TECHNOLOGY (ELECTRONICS)

GUIDELINES FOR PRACTICAL ASSESSMENT TASKS (PAT)

GRADE 12

2022

These guidelines consist of 39 pages.

TABLE OF CONTENTS

| | PAGE |
|--|-------------|
| 1. INTRODUCTION | 3 |
| 2. TEACHER GUIDELINES | 4 |
| 2.1 How to administer PATs | 4 |
| 2.2 How to mark/assess PATs | 4 |
| 2.3 PAT Programme of Assessment (PAT PoA) | 5 |
| 2.4 Moderation of PATs | 6 |
| 2.5 Absence/Non-submission of tasks | 6 |
| 2.6 Simulations | 7 |
| 2.7 Projects | 7 |
| 2.8 Working Mark Sheet | 8 |
| 3. LEARNER GUIDELINES | 9 |
| 3.1 PAT 2022 cover page | 9 |
| 3.2 Instructions to learners | 10 |
| 3.2 Declaration of Authenticity (Compulsory) | 10 |
| 4. SIMULATIONS | 11 |
| 4.1 Simulation 1: RLC series circuit | 11 |
| 4.2 Simulation 2: Non-inverting op-amp | 14 |
| 4.3 Simulation 3: Switching circuits using a 555 IC and a 741 op-amp | 19 |
| 4.4 Simulation 4: Common emitter amplifier | 24 |
| 5. SECTION B: DESIGN AND MAKE | 29 |
| 5.1 Design and make: Part 1 | 30 |
| 5.2 Assessment of the design and make phase: Part 1 | 32 |
| 5.3 Design and make: Part 2 | 34 |
| 5.4 Assessment of design and make phase: Part 2 | 35 |
| 6. PROJECTS | 36 |
| 6.1 Practical project 6.1: Sound-to-light controller | 36 |
| 6.2 Practical project 6.2: Dual voltage power supply | 38 |
| 6.3 Practical project 6.3: Electronic piano | 39 |
| 7. CONCLUSION | 39 |

1. INTRODUCTION

The 18 Curriculum and Assessment Policy Statements subjects which contain a practical component all include a practical assessment task (PAT). These subjects are:

- **AGRICULTURE:** Agricultural Management Practices, Agricultural Technology
- **ARTS:** Dance Studies, Design, Dramatic Arts, Music, Visual Arts
- **SCIENCES:** Computer Applications Technology, Information Technology, Technical Sciences; Technical Mathematics
- **SERVICES:** Consumer Studies, Hospitality Studies, Tourism
- **TECHNOLOGY:** Civil Technology, Electrical Technology, Mechanical Technology and Engineering Graphics and Design

A practical assessment task (PAT) mark is a compulsory component of the final promotion mark for all candidates offering subjects that have a practical component and counts 25% (100 marks) of the end-of-the-year examination mark. The PAT is implemented across the first three terms of the school year. This is broken down into different phases or a series of smaller activities that make up the PAT. The PAT allows for learners to be assessed on a regular basis during the school year and it also allows for the assessment of skills that cannot be assessed in a written format, e.g. test or examination. It is therefore important that schools ensure that all learners complete the practical assessment tasks within the stipulated period to ensure that learners are resulted at the end of the school year. The planning and execution of the PAT differs from subject to subject.

Practical assessment tasks are designed to develop and demonstrate a learner's ability to integrate a variety of skills in order to solve a problem. The PAT also makes use of a technological process to inform the learner what steps need to be followed to derive a solution for the problem.

The PAT consists of four simulations and a practical project. The teacher may choose any ONE of the practical projects and any TWO simulations available for ELECTRONICS.

The teacher must apply assessment on an ongoing basis at the same time that the learner is developing the required skills. TWO simulations should be completed by the learners, in addition to the manufacturing of a practical project.

The PAT incorporates all the skills the learner has developed throughout the year. The PAT ensures that all the different skills will be acquired by learners on completion of practical work, as well as the correct use of tools and instruments.

Requirements for presentation

A learner must present the following:

- PAT file with all the evidence of simulations, design and prototyping. A copy of the PAT 2022 cover page. The relevant simulations and assessment sheets should be copied and handed to each learner to include in the file.
- Practical project with:
 - Enclosure:
 - The file must include a design.
 - The enclosure and the design must match.
 - No cardboard boxes are allowed.
 - Plastic, wooden and metal enclosures are acceptable.
 - Enclosures that are manufactured and/or assembled by the learners are preferred.
 - The enclosure should be accessible for scrutiny inside.
 - Lids that are secured are preferred.

- Circuit board:
 - The file should include the PCB design.
 - The PCB must be mounted inside the enclosure in such a manner that it can be removed for scrutiny. Alternatively, inspection can be made from the bottom in cases where translucent (see-through) enclosures are used.
 - Switches, potentiometers, connectors and other items must be mounted.
 - Wiring must be neat and bound/wrapped.
 - Wiring must be long enough to allow for the PCB to be removed and inspected with ease.
- Logo and name:
 - The file should contain the logo and name design and specification plate.
 - Logo, specification plate and name must be prominent on the enclosure.
 - The logo/specification plate must be affixed in a permanent manner – painted, glued or stuck on with vinyl

The PAT will have a financial impact on the school's budget and school management teams are required to make provision to accommodate this particular expense.

PAT components and other items must be acquired timeously, for use by the learners, before the end of the first term at the start of the academic year.

It is the responsibility of the HOD to ensure that the teacher is progressing with the PAT from the start of the school year.

Provincial departments are responsible for setting up moderation timetables and consequently PATs should be completed in time for moderation.

2. TEACHER GUIDELINES

2.1 How to administer PATs

Teachers must ensure that learners complete the simulations required for each term. The project should be started in January in order to ensure its completion by August. In instances where formal assessments take place, the teacher has to assume responsibility therefore.

The PAT should be completed during the **FIRST THREE TERMS** and must be ready at the start of PAT moderation. Teachers must make copies of the relevant simulations and hand them to learners at the beginning of each term.

The PAT must not be allowed to leave the workshop and must be kept in a safe place at all times when learners are not working on them.

The weightings of the PAT must be adhered to and teachers are not allowed to change weightings for the different sections.

2.2 How to mark/assess the PATs

The PAT for Grade 12 will be set and assessed internally, but moderated externally. All formal assessment will be done by the teacher.

The teacher is required to produce a **working model and model answer file** that sets the baseline for assessment at a Highly Competent Level for every project choice exercised by the learners. This file must include all the simulations with answers the teacher has done him/herself. The teacher will use the model answers and project to assess the simulations and projects of the learners.

Once a facet sheet has been completed by the teacher, assessment will be deemed to be complete. **No re-assessment will be done once the facet sheets have been completed** and captured by the teacher. Learners must ensure that the work is done to the required standard before the teacher finally assesses the PAT during each stage of completion.

2.3 PAT Programme of Assessment (PAT PoA)

The programme of assessment (PoA) for the PAT is as follows:

| TIME FRAME | ACTIVITY | RESPONSIBILITY |
|------------------------|--|---|
| | Preparation for PAT 2022 | Teacher – Builds the models and works out the model answers for the simulations for 2022. Identifies shortages in tools, equipment and consumable items for simulations that must be procured in 2022. SMT – Receives procurement requests from teachers and processes payments for the acquisition of required items |
| January–March 2022 | Simulation 1 | Teacher – Copies and hands out simulations Learners – Complete simulations Teacher – Assesses simulations HOD – Checks if tasks have been completed and marked by the teacher before the holiday |
| January 2022 | PAT project – procurement | Teacher – Obtains quotations for PAT projects Principal – Approves PAT procurement for PAT projects Teacher – Ensures that PAT projects are ordered and delivered HOD – Checks in on teacher to see if the process is adhered to |
| February 2022 | PAT project – learners commence with project | Teacher – Ensures that there is secure storage for PAT projects Teacher – Hands out and takes in PAT projects Teacher – Includes practical sessions for learners to complete the PAT project every week Learners – Commence with completion of the PAT project HOD – Checks in on teacher to ensure that practical workshop sessions take place on a weekly basis |
| April–June 2022 | Simulation 2 | Teacher – Copies and hands out simulations Learners – Complete simulations Teacher – Assesses simulations HOD – Checks if tasks have been completed and marked by the teacher before the holiday |
| April–June 2022 | Moderation of Simulation 1 | District subject facilitator/subject specialist will visit the school and moderate simulation 1 10% of learners' work is moderated |
| April–June 2022 | PAT project – learners continue with project | Teacher – Ensures that there is secure storage for PAT projects Teacher – Hands out and takes in PAT projects Teacher – Includes practical sessions for learners to complete the PAT project every week Learners – Continue with completion of the PAT project HOD – Checks in on teacher to ensure that practical workshop sessions take place on a weekly basis |
| July holidays 2022 | PAT intervention | Learners that are behind on the PAT are required to complete the project during this holiday. |
| July–August 2022 | Moderation of Simulation 2 | District subject facilitator/subject specialist will visit the school and moderate simulation 2 – different learners from the previous term 10% of learners' work is moderated |
| July–August 2022 | PAT project – completion | Teacher – Ensures that there is secure storage for PAT projects Teacher – Hands out and takes in PAT projects Teacher – Completes the PAT project with learners and compiles the PAT file Learners – Complete the PAT project and file HOD – Checks to see that 100% of the PAT files and projects are completed and assessed |
| September–October 2022 | PAT moderation | PAT projects are moderated by subject facilitators/subject specialists from the province and learners are available to demonstrate skills 10% of learners are moderated randomly |

2.4 Moderation of PATs

Provincial moderation of each term's simulations will start as early as the following term. Simulation 1 should be moderated as soon as the second term starts. Similarly, Simulation 2 will be moderated in July. The project will, however, only be moderated on completion.

During moderation of the PAT the learner's file and project must be presented to the moderator.

The moderation process is as follows:

- During moderation, learners are randomly selected to demonstrate the different simulations. Both simulations will be moderated.
- **The teacher is required to build a model of each project chosen for the school.**
- **This model must be on display during moderation.**
- **The teacher's model forms the standard of the moderation at Level 4 (Highly Competent).**
- **Level 5 assessments must exceed the model of the teacher in skill and finishing.**
- Learners who are moderated will have access to their files during moderation and may refer to the simulations they completed earlier in the year.
- Learners may NOT ask assistance from other learners during moderation.
- All projects and files must be on display for the moderator.
- **If a learner is unable to repeat the simulation or cannot produce a working circuit during moderation, marks will be deducted and circuits assessed as not being operational.**
- The moderator will randomly select no fewer than **two projects** (not simulations) and the learners involved will have to explain how the project was manufactured.
- Where required, the moderator should be able to call on the learner to explain the function and principles of operation, and request the learner to exhibit the skills acquired through the simulations for moderation purposes.
- On completion the moderator will, if needed, adjust the marks of the group upwards or downwards, depending on the outcome of moderation.
- Normal examination protocols for appeals will be adhered to, if a dispute arises from adjustments made.

2.5 Absence/Non-submission of Tasks

The absence of a PAT mark in Electrical Technology without a valid reason: The learner will be given three weeks before the commencement of the final end-of-year examination to submit outstanding task. Should the learner fail to fulfil the outstanding PAT requirement, such a learner will be awarded a zero (0) for that PAT component.

2.6 Simulations

Simulations are circuits, experiments and tests/tasks which the learner will have to build, test and measure and practically do as part of the development of practical skills. These skills have to be illustrated to the external moderator that visits the school at intervals during the school year.

Teachers who use simulation programs on a computer may use them for the learners to practice on. However, it is required that the circuit be built using real components and that measurements be made with actual instruments for the purposes of assessment and moderation.

The correct procedure for completing simulations is outlined below for teachers and school management teams who are responsible for the implementation of the PAT in Electrical Technology.

- STEP 1: The teacher will choose simulations from the provided examples.
- STEP 2: Compile a list of the components needed for every simulation. Add extra components as these items are very small and you will need extras, as these items are lost/damaged very easily when learners work with them.
- STEP 3: Contact three different electronics component suppliers for comparative quotations.
- STEP 4: Submit the quotations to the SMT for approval and procurement of the items.
- STEP 5: Place the components in storage. Collate items for each simulation, thus making it easier to distribute and use during practical sessions. Ensure that different values of components do not mix, as this would lead to components being used incorrectly and this could damage the component and in extreme cases, the equipment used.
- STEP 6: Copy the relevant simulations and hand them out to learners at the start of the term.

Teachers are allowed to adjust circuits and component values to suit their environment/resource availability.

Teachers are required to develop a set of model answers in the teacher's file.

Moderators will use the teacher's model answers and artefacts when moderating.

2.7 Projects

The projects are construction projects teachers can choose for their learners. These projects are based on proven circuits provided from schools and subject advisors. The projects are based on working prototypes and require careful construction in order for them to operate correctly.

Projects vary in cost and teachers must ensure that the projects chosen fall within the scope of the school's budget.

Once the teacher has decided on a circuit, he/she must construct the prototype. Thereafter, copies of the provided circuit can be made and distributed to learners. They **MUST** redraw these circuits in their portfolios correctly.

The description of the operation of the circuits is **NOT** complete. Learners are required to interrogate the function of the components in the provided circuit. They should elaborate on the purpose of components in the circuit. It is recommended that learners investigate similar circuits available on the internet and in the school library or workshop reference books.

2.8 Working mark sheet

(A working Excel file is provided with this PAT)

| PAT mark sheet | | Term 1 | Term 2 | Project | | Total = Term 1 + Term 2 + Project 250 | Mark out of 100 | Moderated Mark |
|----------------|-----------------|--------------------|--------------------|--|------------------------------------|---|-----------------|----------------|
| No. | Name of Learner | Simulation 1 50 | Simulation 2 50 | Design and Make Part 1 120 | Design and Make Part 2 30 | | | |
| 1 | | | | | | | | |
| 2 | | | | | | | | |
| 3 | | | | | | | | |
| 4 | | | | | | | | |
| 5 | | | | | | | | |
| 6 | | | | | | | | |
| 7 | | | | | | | | |
| 8 | | | | | | | | |
| 9 | | | | | | | | |
| 10 | | | | | | | | |
| 11 | | | | | | | | |
| 12 | | | | | | | | |
| 13 | | | | | | | | |
| 14 | | | | | | | | |
| 15 | | | | | | | | |
| | Total | | | | | | | |
| | Average | | | | | | | |

Teacher Name: _____

Principal Name: _____

Moderator Name: _____

Signature: _____

Signature: _____

Signature: _____

Date: _____

Date: _____

Date: _____

3. LEARNER GUIDELINES

PAT 2022 cover page (Place this page at the front of the PAT.)

**Department of Basic Education
Grade 12
CAPS for Technical High Schools
Practical Assessment Task – Electrical Technology**

Time allowed: Terms 1–3 (2022)

Learner Name: _____

Class: _____

School: _____

Specialisation: ELECTRONICS**Complete TWO simulations.****Project (Write the name of the project):** _____**Evidence of moderation:****NOTE:**

When the learner evidence (LE) selected has been moderated at school level, the table will contain evidence of moderation. Provincial moderators will sign the provincial moderation and only sign if re-moderation is needed.

| Moderation | Signature | Date | Signature | Date |
|-----------------------|-----------|------|---------------|------|
| School-based | | | | |
| District moderation | | | | |
| Provincial moderation | | | Re-moderation | |

Mark allocation

| PAT Component | Maximum Mark | Learner Mark | Moderated Mark |
|-------------------------------------|--------------|--------------|----------------|
| Simulation 1 | 50 | | |
| Simulation 2 | 50 | | |
| Design and Make Project – Circuit | 120 | | |
| Design and Make Project – Enclosure | 30 | | |
| Total | 250 | | |

3.1 Instructions to learner

- The practical assessment task counts 25% of your final promotion mark.
- All work produced by you must be your own effort. Group work is NOT allowed.
- The practical assessment task must be completed over three terms.
- The PAT file must contain TWO simulations and a practical project.
- Calculations should be clear and include units. Calculations should be rounded off to TWO decimals. SI units should be used.
- Circuit diagrams can be hand-drawn or drawn on CAD. NO photocopies or scanned files are allowed.
- Photos are allowed and may be in colour or greyscale. Scanned photos and photocopies are allowed.
- Learners with identical photos will be penalised and receive zero for that section.
- This document must be placed inside your PAT file together with the other evidence.

3.2 Declaration of Authenticity (COMPULSORY)

Declaration:

I _____ (Name) herewith declare that the work represented in this File/evidence is entirely my own effort. I understand that if proven otherwise, my final results may be withheld.

Signature of learner

Date

4. SIMULATIONS**4.1 Simulation 1: RLC series circuit**

| | | |
|------------------------|----------------------------|---|
| Name of learner: _____ | | Mark <div style="border: 1px solid black; width: 60px; height: 60px; margin: 0 auto; display: flex; align-items: center; justify-content: center;"> — 50 — </div> |
| Class: _____ | Date Completed: _____ | |
| Date Assessed: _____ | Assessor Signature: _____ | |
| Date Moderated: _____ | Moderator Signature: _____ | |

4.1.1 Purpose:

- To understand the operation of a resistor, inductor and capacitor in a series circuit with an AC supply.
- To understand resonant frequency.
- To compare the measured and the calculated values.

4.1.2 Procedure:

Build the series RLC circuit in FIGURE 4.1.4 on the breadboard using the components provided.

Connect the circuit to a function generator.

Set the output signal voltage of the function generator to 5 V with a frequency of 50 kHz.

Take the measurements as asked in TABLE 4.1.5 with the frequency adjusted to 50 Hz, 159 Hz and 500 Hz and then answer the questions that follow.

4.1.3 Required resources:

| COMPONENTS | TOOLS AND EQUIPMENT |
|---|---|
| $R_1 = 100 \Omega$ resistor $L_1 = 10 \mu\text{H}$ inductor $C_1 = 100 \mu\text{F}$ capacitor | Multimeter Function generator Leads Breadboard Side cutters Pair of pliers Oscilloscope |

4.1.4 **Circuit Diagram:**

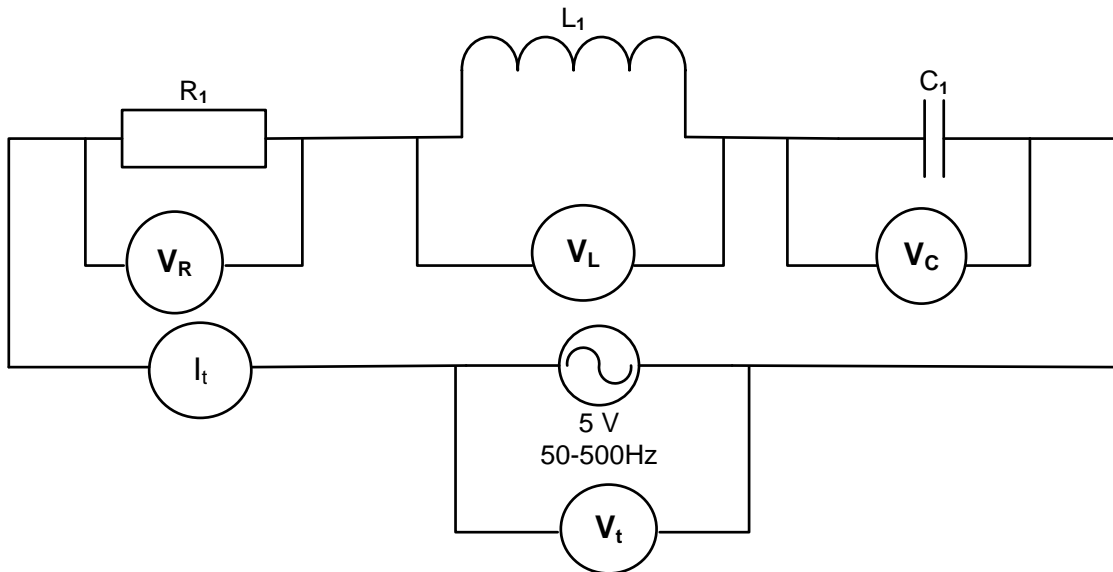


FIGURE 4.1.4: RLC CIRCUIT DIAGRAM

4.1.5 Complete TABLE 4.1.5 by entering measured values of V_R , V_L , V_C , V_T and I_T .
NOTE: Alternatively measure with the oscilloscope and convert to V_{rms} values.

| METERS CONNECTED ACROSS | MEASUREMENTS AT 50 Hz | MEASUREMENTS AT 159 Hz | MEASUREMENTS AT 500 Hz |
|-------------------------|-----------------------|------------------------|------------------------|
| V_R | | | |
| V_L | | | |
| V_C | | | |
| V_T | | | |
| I_T | | | |

TABLE 4.1.5

(13)

4.1.6 Study the measurements in TABLE 4.1.5 above and answer the following:

(a) Compare the values of V_L and V_C at 50 Hz.

(2)

(b) Calculate the values of X_L and X_C at 50 Hz with:

(4)

$$X_L = 2\pi fL$$

$$X_C = \frac{1}{2\pi fC}$$

$X_L =$ _____

$X_C =$ _____

(c) Compare the values of V_L and V_C at 500 Hz. (2)

(d) Calculate the values of X_L and X_C at 500 Hz. (4)

$X_L =$ _____ $X_C =$ _____

(e) Compare the values of V_L and V_C at 159 Hz. (2)

(f) Calculate the values of X_L and X_C at 159 Hz (4)

$X_L =$ _____ $X_C =$ _____

(g) Calculate the resonant frequency. (3)

4.1.7 Write a conclusion about the measurements in 4.1.5 and calculations in 4.1.6 when the circuit is at resonance. (4)

RUBRIC FOR SIMULATION 1

| LEVEL DESCRIPTOR | | | | MARKS OBTAINED |
|--|---|--|--|----------------|
| 0 | 1 | 2 | 4 | |
| The learner was not able to build the circuit on his own. | The learner was able to partially build the circuit on his own. | The learner was able to correctly build the circuit with the assistance of the teacher. | The learner built the circuit correctly without the assistance of the teacher. | |
| The learner was not able to connect the measuring instruments. | The learner was able to partially connect the measuring instruments to the circuit. | The learner connected the measuring instruments correctly and measured the voltages and currents with the assistance of the teacher. | The learner connected the measuring instruments correctly and measured the voltages and currents on his own. | |

(12)

Total: [50]

4.2 Simulation 2: Non-inverting op-amp

| | | |
|------------------------|----------------------------|--|
| Name of learner: _____ | | Mark <div style="border: 1px solid black; width: 60px; height: 60px; margin: 0 auto; display: flex; align-items: center; justify-content: center;"> 50 </div> |
| Class: _____ | Date Completed: _____ | |
| Date Assessed: _____ | Assessor Signature: _____ | |
| Date Moderated: _____ | Moderator Signature: _____ | |

4.2.1 Purpose:

- To construct a simple circuit using a 741 op-amp to build a non-inverting amplifier and display the input and output waveforms on an oscilloscope.

4.2.2 Required resources:

| TOOLS/INSTRUMENTS | MATERIALS |
|--|--|
| Analogue/Digital trainer Analogue/Digital oscilloscope Function generator Variable DC power supply Side cutters Wire stripper Multimeter | 1 x LM 741 op-amp 2 x 10 kΩ for Ra and Rb Connecting wires |

4.2.3 Procedure:

- (a) Construct the circuit on the breadboard as shown in FIGURE 4.2.3.

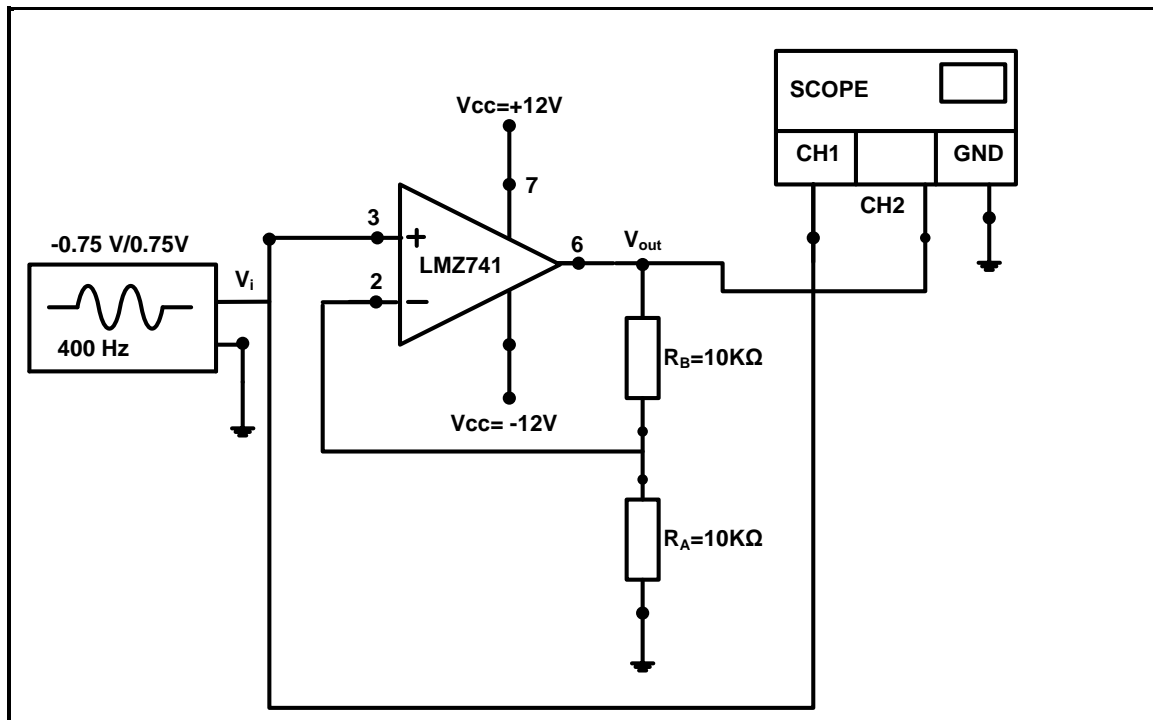


FIGURE 4.2.3: NON-INVERTING OP AMP

- (b) The value of CH1 is set on 0,5 V/division and 1 V/division for CH2 and the time must be set on 1 ms/division.
- (c) Measure the input and output voltage with the oscilloscope and record the values below. All values measured with the oscilloscope are peak-to-peak.

$$\text{Voltage} = \frac{V_{out}(p-p)}{V_{in}(P-P)}$$

= _____

= _____

(2)

- (d) Use the formula below to determine the voltage gain of the circuit.

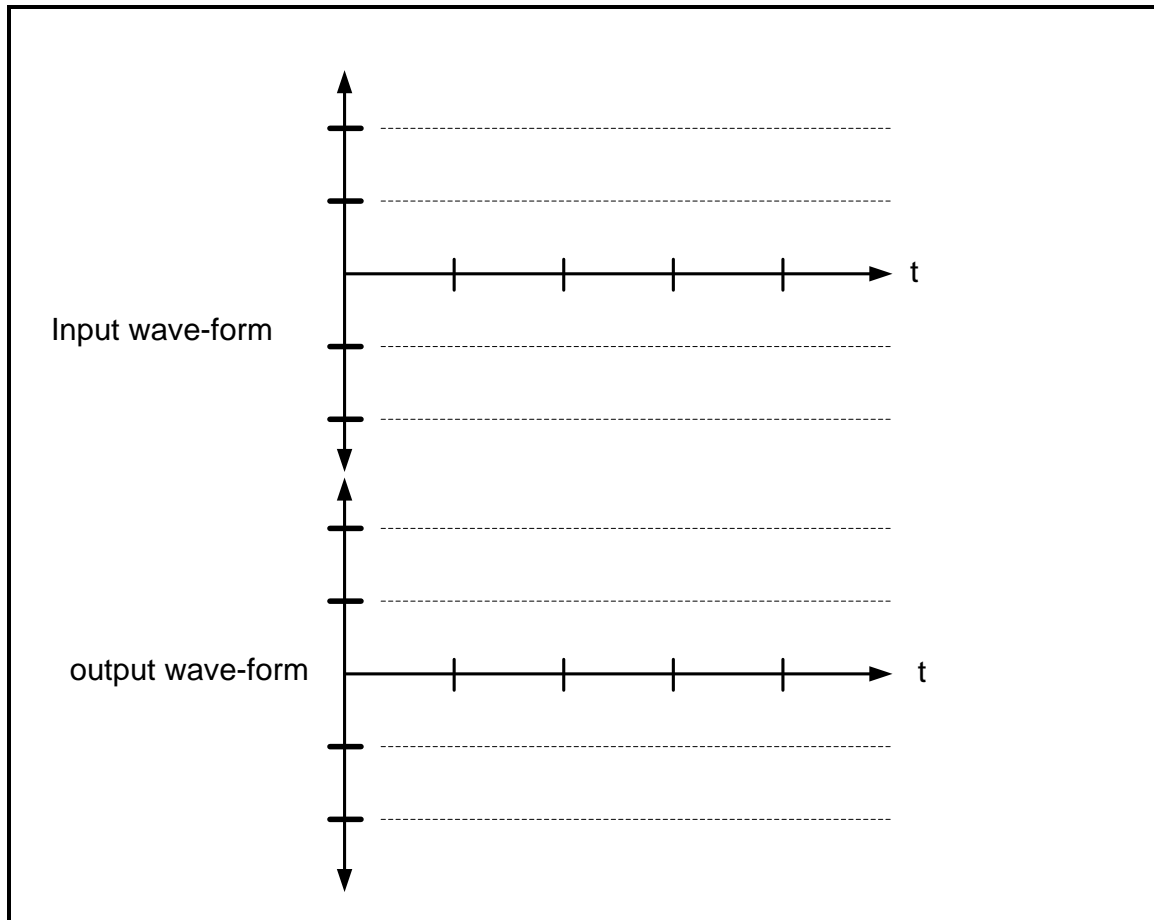
$$\text{Voltage gain} = 1 + \frac{R_B}{R_A}$$

= _____

= _____

(2)

- (e) Draw the input and output waveforms for at least TWO complete cycles in the table below.



(6)

- (f) Measure and record the voltage across R_B and output voltage values in the table below. Also calculate the voltage gain values in the table below as you change the value of R_B in the circuit.

| RESISTOR R_B | V_{RB} | V_{OUT} | VOLTAGE GAIN |
|-------------------|----------|-----------|--------------|
| (a) 15 k Ω | | | |
| (b) 22 k Ω | | | |
| (c) 33 k Ω | | | |
| (d) 47 k Ω | | | |
| (e) 56 k Ω | | | |
| (f) 82 k Ω | | | |

(18)

TABLE 1.5

RUBRIC FOR SIMULATION 2

| | | |
|--|---|--|
| Learner was able to construct a minimum part of the circuit correctly without assistance | Learner was able to construct a part of the circuit correctly without assistance. | Learner was able to construct the circuit correctly without assistance |
| 1 | 3 | 4 |

(4)

4.2.4 **Conclusion:**

(2)

FACET SHEET FOR SIMULATION 2: CONSTRUCTION OF THE NON-INVERTING OP-AMP

| | FACET 1 | FACET 2 | FACET 3 | FACET 4 | MAXIMUM POSSIBLE MARKS | LEARNER'S MARK |
|--|---------------------------------------|--|--|--|-------------------------------|-----------------------|
| Prepare for the simulation | Identifies component correctly (1) | Collects the PSU/Mini trainer (1) | Collects instruments (1) | Collects hand tools (1) | (4) | |
| Correct connection breadboards – nodes and polarity | 6 nodes connected correctly (1) | Correct connection on the oscilloscope. (1) | Correct connection on the op-amp. (1) | Correct connection on the resistors (1) | (4) | |
| Circuit | Circuit not working (0) | | | Circuit working correctly (4) | (4) | |
| Housekeeping | Never (0) | Reminded (2) | Sometimes (3) | Always (4) | (4) | |
| SECTION B: | | | | | 16 | |
| SECTION A: | | | | | 34 | |
| TOTAL MARK: | | | | | 50 | |

4.3 Simulation 3: Switching circuits using a 555 IC and a 741 op-amp

| | | | | | | |
|------------------------|----------------------------|--|------|-------|--|----|
| Name of learner: _____ | | <table border="1" style="margin: auto;"> <tr> <td style="padding: 5px;">Mark</td> <td style="text-align: center; width: 100px;">_____</td> </tr> <tr> <td></td> <td style="text-align: center;">50</td> </tr> </table> | Mark | _____ | | 50 |
| Mark | _____ | | | | | |
| | 50 | | | | | |
| Class: _____ | Date completed: _____ | | | | | |
| Date Assessed: _____ | Assessor Signature: _____ | | | | | |
| Date Moderated: _____ | Moderator Signature: _____ | | | | | |

Simulation 3A: Monostable multivibrator using 555 IC

4.3.1 Purpose:

- To build the monostable multivibrator in FIGURE 4.3.3 using a 555 IC.
- To compare the theory learned in class with the actual circuit.

4.3.2 Required Resources:

| TOOLS/INSTRUMENTS | MATERIALS |
|------------------------|---|
| Experiment board | 1 x 555 IC |
| Voltmeter (multimeter) | 2 x 10 kΩ resistors |
| DC power supply, 5 V | 1 x 1 kΩ resistors |
| Side cutters | 2 x 470 Ω resistors |
| Long-nose pliers | 1 x 220 μF electrolytic capacitor, 16 V |
| Wire stripper | 1 x 220 μF electrolytic capacitor, 16 V |
| | 1 x LED |
| | 1 x push button/tactile switch |
| | Connecting wires |

4.3.3 Procedure:

Build the circuit diagram in FIGURE 4.3.3 on your experiment board.
 After the teacher has checked the circuit, switch the power ON.
 Connect a multimeter to measure the voltage on pin 2.
 Connect a multimeter to measure the voltage across C₁.

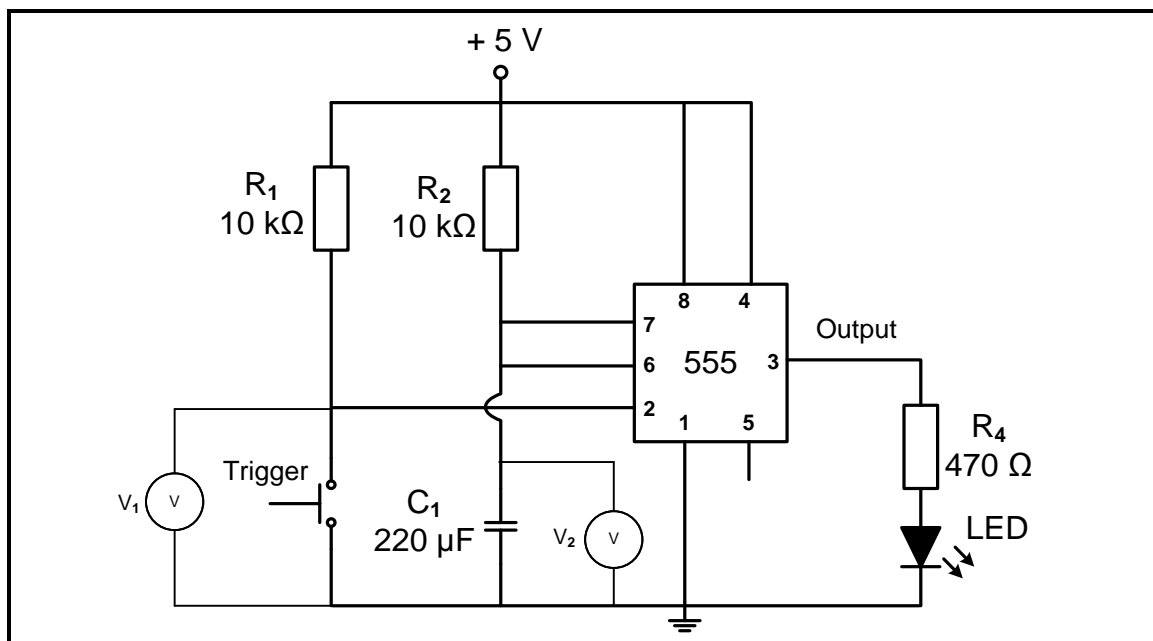


FIGURE 4.3.3: 555 MONOSTABLE MULTIVIBRATOR

(a) Write down the voltage measured across pin 2.
Voltage across pin 2 $V_1 =$ _____ (1)

(b) State the function of R_1 with reference to pin 2 and the output. (2)

(c) Press the trigger input and observe what happens to the voltage measurement across the capacitor. Write down the voltage measured across C_1 just before the LED switches OFF (maximum charged voltage).
Voltage across C_1 . $V_2 =$ _____ (1)

(d) Compare the voltage across C_1 to the supply voltage. (2)

(e) Press the trigger input twice within a short time frame to simulate switch bounce. Write down your observation. (3)

(f) Replace capacitor C_1 with a 100 μF capacitor. Switch ON the circuit, press the trigger input and observe. Write down your observation and give a reason why this happens. (4)

(g)

| | | |
|---|---|---|
| Learner was able to construct a minimum part of the circuit correctly without assistance. | Learner was able to construct a part of the circuit correctly without assistance. | Learner was able to construct the circuit correctly without assistance. |
| 1 | 3 | 4 |

(4)

Simulation 3A: (17)

Simulation 3B: Inverting op-amp using 741 IC**4.3.4 Purpose:**

- To build the inverting amplifier circuit in FIGURE 4.3.6(a) using a 741 op-amp and display the output waveforms on an oscilloscope.
- To investigate the effect of ratio R_F to R_{IN} on the gain and the output of the amplifier.

4.3.5 Required Resources:

| TOOLS/INSTRUMENTS | MATERIALS |
|------------------------------|-----------------------------|
| Function generator | 1 x LM741 op-amp |
| Dual-trace oscilloscope | 1 x 100 k Ω resistor |
| +9 V 0 V–9 V DC power supply | 1 x 68 k Ω resistor |
| Side cutters | 1 x 47 k Ω resistor |
| Wire stripper | 1 x 22 k Ω resistor |
| Calculator | 1 x 10 k Ω resistor |
| | Connecting wires |

4.3.6 Procedure:

Set the dual voltage power supply to +9 V/-9 V.

Set the function generator to deliver a 0,5 V peak 1 kHz sine wave.

Build the circuit in FIGURE 4.3.6(a) on your experiment board and connect it to the supply and input.

Connect channel 1 of the oscilloscope across the input to display at least TWO complete cycles.

Connect channel 2 of the oscilloscope across the output to display at least TWO complete cycles.

(a) Build the circuit in FIGURE 4.3.6(a) on the experiment board.

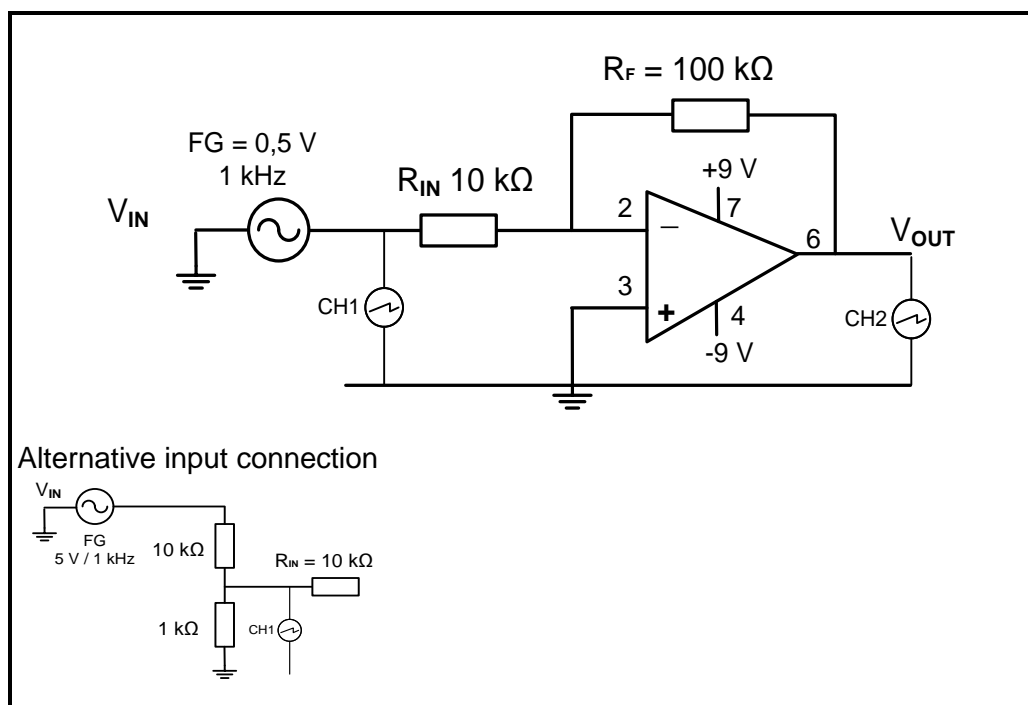
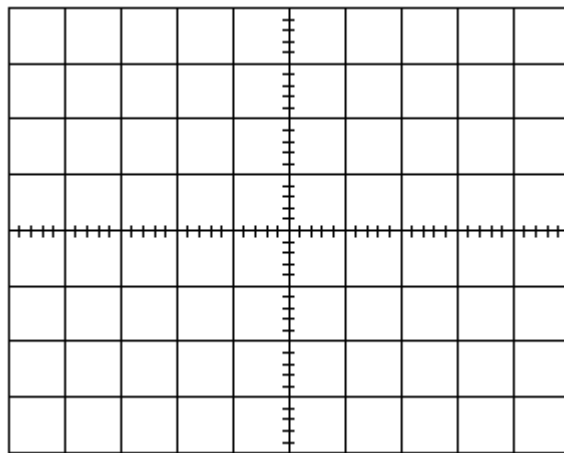


FIGURE 4.3.6 (a): 741 INVERTING OP-AMP

- (b) Draw the input and output waveforms on the oscilloscope grid provided in OSCILLOGRAM 4.3.6(b) below.



V/Div: _____ (Ch 1)

V/Div: _____ (Ch 2)

T/Div: _____

NOTE: 1 mark for each correctly drawn waveform. 1 mark for each correct oscilloscope setting.

OSCILLOGRAM 4.3.6(a)

(5)

- (c) Use the oscilloscope settings to determine the values of:

$V_{IN} =$ _____

(1)

$V_{OUT} =$ _____

(1)

- (d) Calculate the gain of the amplifier using the determined voltage values.

(3)

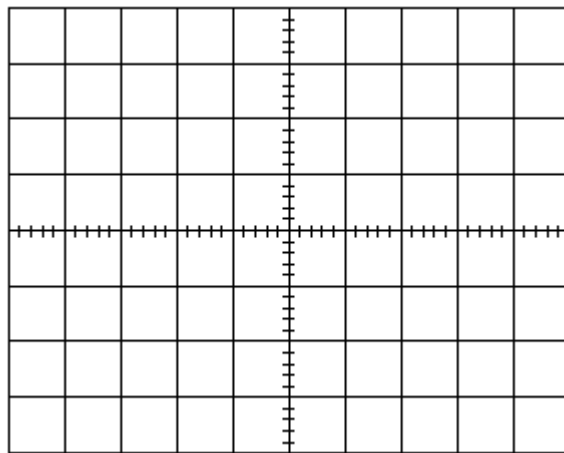
- (e) Replace resistor R_F 100 k Ω with the following resistors and write down the value of the output voltage.

| R_F | OUTPUT VOLTAGE |
|---------------|----------------|
| 68 k Ω | |
| 47 k Ω | |
| 22 k Ω | |
| 10 k Ω | |

TABLE 4.3.6(e)

(4)

- (f) Draw the input and output waveforms observed on the oscilloscope grid below when R_F is 10 k Ω in OSCILLOGRAM 4.3.6(f).



V/Div: _____ (Ch 1)

V/Div: _____ (Ch 2)

T/Div: _____

NOTE: 1 mark for each correctly drawn waveform. 1 mark for each correct oscilloscope setting.

OSCILLOGRAM 4.3.6(f)

(5)

- (g) Calculate the gain of the amplifier when $R_F = 10$ k Ω .

(3)

- (h) Compare the output voltages in TABLE 4.2.6(e) to the input voltage in (c) and write a conclusion.

(3)

| 1 | 3 | 4 |
|---|---|---|
| Learner was able to construct a minimum part of the circuit correctly without assistance | Learner was able to construct a part of the circuit correctly without assistance. | Learner was able to construct the circuit correctly without assistance |
| Learner was able to connect the oscilloscope probes correctly but could not set it up to display the signals. | Learner was able to connect the oscilloscope probes correctly and partially set it up to display the signals. | Learner was able to connect the oscilloscope probes correctly and set it up to display the signals correctly. |

(8)

Simulation 3B: (33)

Subtotal simulation 3A: (17)

Subtotal simulation 3B: (33)

TOTAL SIMULATION 3: [50]

4.4 Simulation 4: Common emitter amplifier

| | | |
|------------------------|----------------------------|---------------|
| Name of learner: _____ | | Mark _____ |
| Class: _____ | Date completed: _____ | |
| Date Assessed: _____ | Assessor Signature: _____ | |
| Date Moderated: _____ | Moderator Signature: _____ | |

Simulation 4.4A: Common emitter amplifier**4.4.1 Purpose:**

- To construct a potential divider circuit using discrete components.
- To measure/calculate the voltages and currents of the circuit.

4.4.2 Resources required:

| TOOLS/INSTRUMENTS | MATERIALS |
|-------------------------------|--|
| Analogue/Digital trainer | 1 x variable resistor (80–90 k Ω) |
| Analogue/Digital oscilloscope | 1 x 6,8 k Ω resistor |
| Function generator | 1 x 15 k Ω resistor |
| Multimeter | 1 x 1,5 k Ω resistor |
| Variable DC power supply | 1 x 2N4401 NPN transistor or any general-purpose NPN transistor |
| Side cutters | Connecting wires |
| Wire stripper | Microphone |

4.4.3 Procedure:

- (a) Build the circuit in FIGURE 4.4.3 on the breadboard.

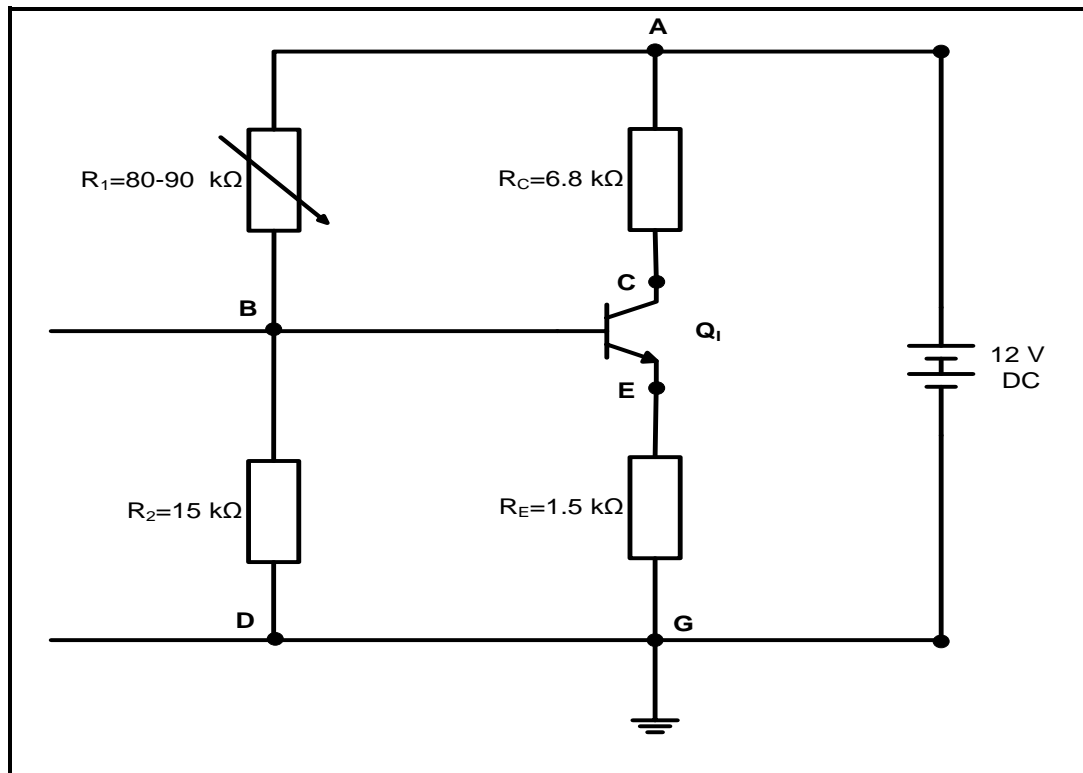


FIGURE 4.4.3: POTENTIAL DIVIDER CIRCUIT

- (b) Measure and record in TABLE 4.4.3(b) the DC voltages for test points A-B, B-G, A-C (V_{RE}), C-E, E-G and C-G.

| TEST POINTS | MEASURED DC VOLTAGES |
|---------------|----------------------|
| A-B | |
| B-G (Q value) | |
| A-C (R_E) | |
| C-E | |
| E-G | |
| B-E | |
| C-G (Q value) | |

(7)

TABLE 4.4.3(b)

- (c) Measure and record the following DC current values using a multimeter:

$I_B =$ _____

(2)

$I_C =$ _____

(2)

- (d) Calculate the DC current gain

(3)

(14)

Activity 4.4B: Construction of the common emitter amplifier

4.4.4 Purpose:

- To construct the common emitter amplifier using discrete components.
- To display the input/output waveforms on an oscilloscope.

4.4.5 Procedure:

Construct the circuit shown below.

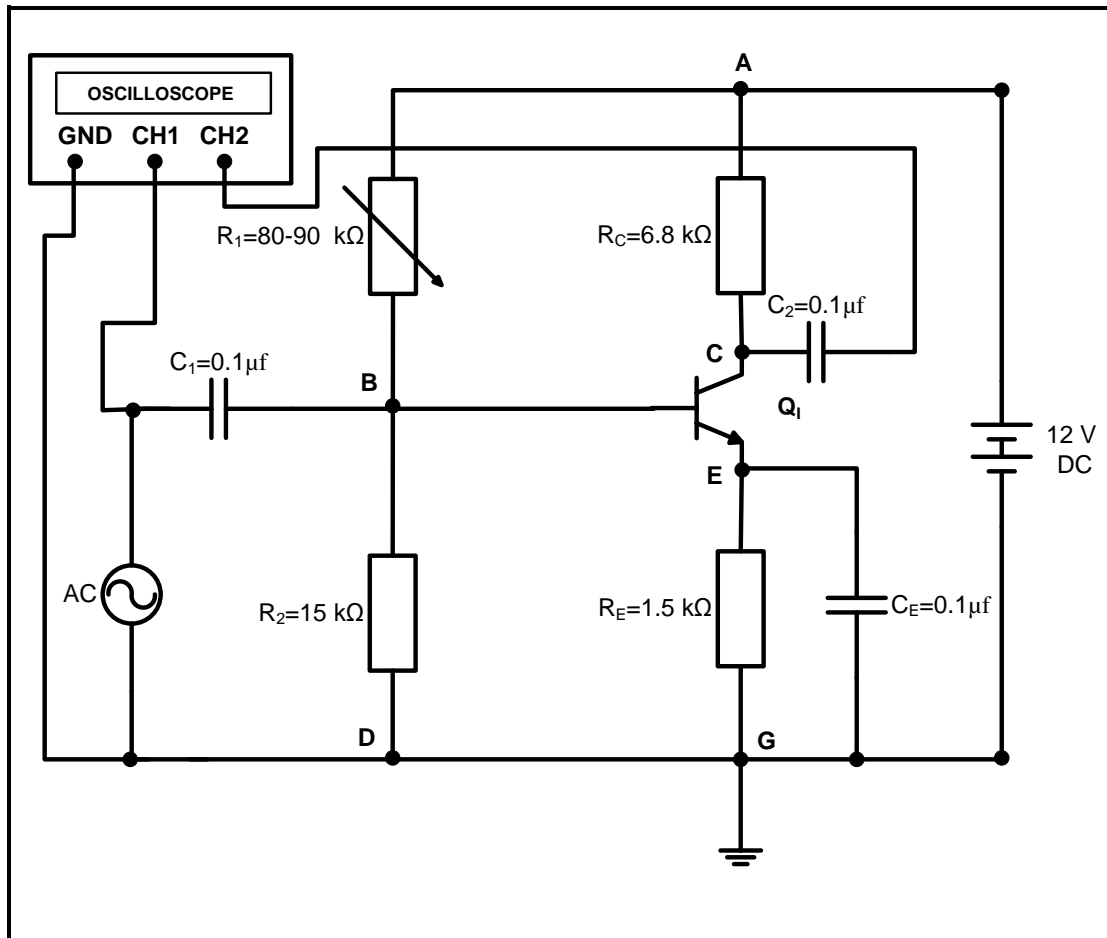


FIGURE 4.4.5: COMMON EMITTER AMPLIFIER

- (a) Calculate the actual capacitance value for C_E if $R_E = 680 \Omega$ and the minimum frequency at which C_E must work = 100 Hertz.

NOTE: If the value you have calculated is not available, use a 25 μf electrolytic capacitor which works for a very wide frequency band.

(3)

- (b) Apply a 1 kHz/10 mV peak-to-peak sine wave from the function generator to the input of the circuit diagram in FIGURE 4.4.5. Use the oscilloscope for the V_{p-p} measurements. Connect the input and output showing the correct phases and amplitude.

(4)

- (c) In FIGURE 4.4.5(c) below measure and draw the input and output voltage waveforms showing the correct phases and amplitude values.

NOTE: If the output signal is distorted, slightly reduce the input signal.

(6)

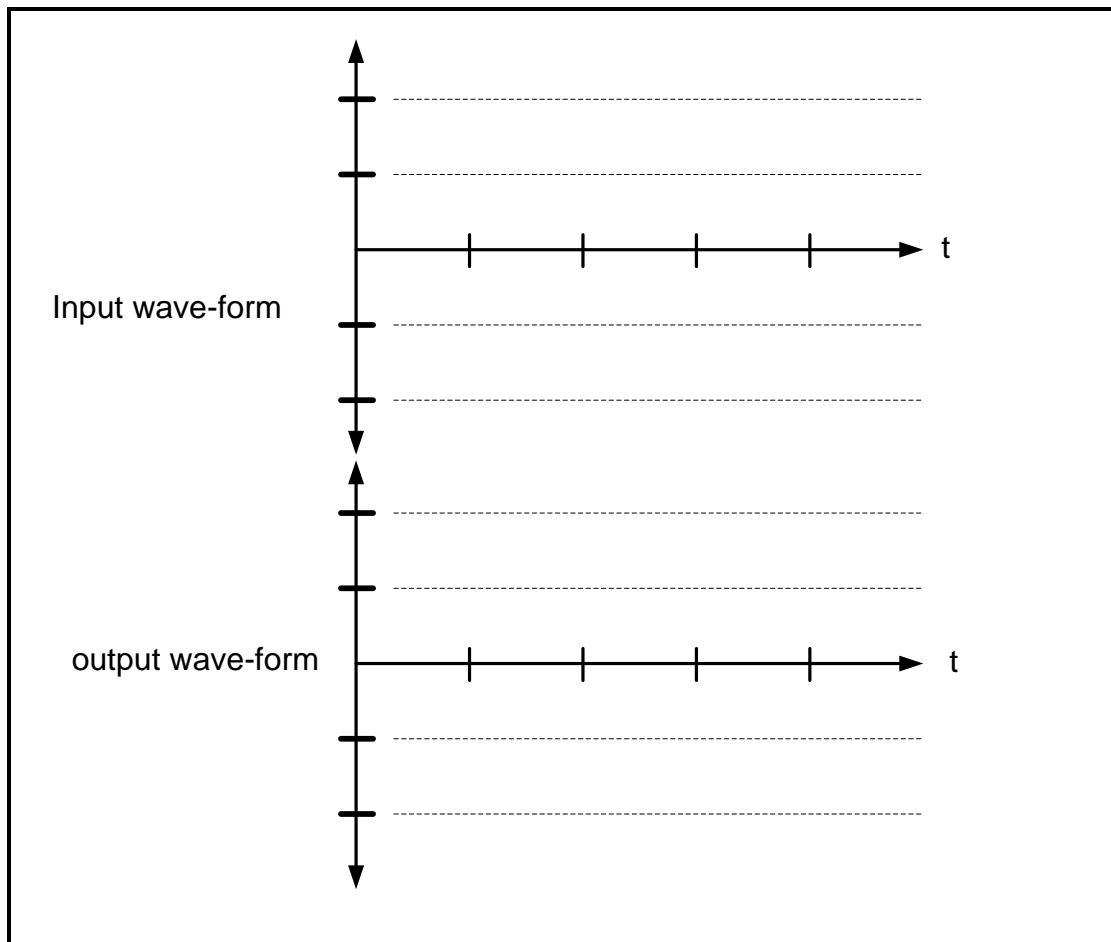


FIGURE 4.4.5(c)

- (d) Calculate the voltage gain from FIGURE 4.4.5(c).

(3)

- (e) What is the phase relation between the output and input waveforms? Explain the reason for this phase relation.

(4)

- (f) Adjust the input signal until the output measures $\pm V_{p-p}$. Connect a multimeter with AC current scale in series with the base to measure the base current.

$I_B =$ _____ (μA)

(2)

(g) Connect the multimeter to measure the collector current by selecting the mA scale.

$I_c =$ _____ (mA) (2)

(h) Calculate the current gain by using the answers in f and g. (4)

(i) Remove the capacitor across the resistor. Measure and record the I_c and V_{out} .

$I_c =$ _____ (mA) (2)

$V_{out} =$ _____ (Vp-p) (2)

(j) What effect does the removal of CE have on collector current and the output voltage? (4)

ACTIVITY 4.4 A: (14)
ACTIVITY 4.4 B: (36)
TOTAL MARK: [50]

5. SECTION B – DESIGN AND MAKE

| Design and Make Project | |
|--------------------------------|------------------------|
| Time: | January to August 2022 |
| Learner Name: | _____ |
| School: | _____ |
| Class: | _____ |
| Title/Type of Project: | _____ |

**INSTRUCTIONS**

- This section is **COMPULSORY** for all learners.
- The teacher will choose a circuit for the project.
- Any project constructed must include at least (but is not limited to):
 - SEVEN components
 - A variety of components (both active and passive)
 - PCB-making in some form
 - Soldering
 - An enclosure with a switch and protection
- The checklist below must be used to ensure that all the required tasks for the PAT have been completed.

PAT CHECKLIST

NOTE: The learner **MUST** complete this checklist for the teacher **BEFORE** marking of that section takes place.

| NO. | DESCRIPTION | TICK (☑) | |
|--------------------------------|--|--------------------------|--------------------------|
| | | NO | YES |
| Design and Make: Part 1 | | | |
| 1. | Circuit diagram drawn | <input type="checkbox"/> | <input type="checkbox"/> |
| 2. | Circuit description completed | <input type="checkbox"/> | <input type="checkbox"/> |
| 3. | Component list completed | <input type="checkbox"/> | <input type="checkbox"/> |
| 4. | Tools list for circuitry populated | <input type="checkbox"/> | <input type="checkbox"/> |
| 5. | Measuring instrument list completed | <input type="checkbox"/> | <input type="checkbox"/> |
| Design and Make: Part 2 | | | |
| 1. | Enclosure design completed and included in the file | <input type="checkbox"/> | <input type="checkbox"/> |
| 2. | Unique name written down and on the enclosure | <input type="checkbox"/> | <input type="checkbox"/> |
| 3. | Logo designed and placed on the enclosure | <input type="checkbox"/> | <input type="checkbox"/> |
| Miscellaneous | | | |
| 1. | Enclosure included in the project | <input type="checkbox"/> | <input type="checkbox"/> |
| 2. | Enclosure prepared and drilled according to the design | <input type="checkbox"/> | <input type="checkbox"/> |
| 3. | Enclosure finished off and completed with name and logo | <input type="checkbox"/> | <input type="checkbox"/> |
| 4. | PCB securely mounted in the enclosure using acceptable techniques | <input type="checkbox"/> | <input type="checkbox"/> |
| 5. | Circuit inside the enclosure is accessible | <input type="checkbox"/> | <input type="checkbox"/> |
| 6. | Internal wiring neat and ready for inspection | <input type="checkbox"/> | <input type="checkbox"/> |
| 7. | File and project completed and ready for moderation at the workshop/room | <input type="checkbox"/> | <input type="checkbox"/> |

5.2 Assessment of the design-and-make phase: Part 1

| NO. | FACET DESCRIPTION | Mark | Achieved = 1 Not achieved = * |
|---|--|-----------|----------------------------------|
| Circuit Diagram | | | |
| 1. | The circuit diagram was drawn using EGD equipment. | 5 | |
| 2. | The circuit diagram was drawn using CAD/any electronic design software. | 1 | |
| 3. | The circuit diagram was drawn using correct symbols. | 3 | |
| 4. | The circuit diagram has all labels – R1, C1, Tr1, etc. | 3 | |
| 5. | The circuit diagram has all component values –100 Ω , 220 μF , etc. | 4 | |
| 6. | The circuit diagram has a name/title. | 2 | |
| 7. | The circuit diagram has a frame and title block. (EGD approach). | 2 | |
| Circuit Diagram Subtotal: | | 20 | |
| Component List | | | |
| 8. | Labels correlate with circuit diagram. | 2 | |
| 9. | Description and values correlate with circuit diagram. | 2 | |
| 10. | Quantities are correct. | 1 | |
| Component List Subtotal: | | 5 | |
| Description of Operation | | | |
| 11. | Basic function of the circuit is described correctly. | 10 | |
| 12. | All subcircuits in the circuit diagram and component list are included in the description. | 5 | |
| 13. | Purposes of subcircuits in the circuit diagram are described correctly. | 5 | |
| 14. | Learner used own interpretation and did not copy from another source verbatim. | 4 | |
| 15. | Sources are acknowledged. | 1 | |
| Description of Operation Subtotal: | | 25 | |
| Tools/Instrument List | | | |
| 16. | The tools/instrument list has been completed. | 4 | |
| 17. | The tools/instruments listed all have a purpose for being used. | 1 | |
| Tools/Instrument List Subtotal: | | 5 | |

| NO. | FACET DESCRIPTION | Mark | Achieved = 1 Not achieved = * |
|------------------------------------|---|-----------|----------------------------------|
| Circuit Board Manufacturing | | | |
| 18. | Transfer of the PCB design onto the blank board is correct. Not over exposed or under exposed. | 5 | |
| 19. | Circuit board is etched neatly according to the PCB design. | 10 | |
| 20. | The learner's name is etched onto the circuit design. | 4 | |
| 21. | All burrs are removed. | 2 | |
| 22. | Axial and radial components are placed neatly and flush with the board. | 5 | |
| 23. | Component orientation are aligned between similar components (e.g. the gold band of all resistors are placed on the same side). | 2 | |
| 24. | Soldered components – leads are cut off, flush and neat on the solder side. | 5 | |
| 25. | More than 60% of the solder joints are shiny (not dry joints). | 5 | |
| 26. | Wire insulation is stripped to the correct length (no extra copper showing). | 3 | |
| 27. | Wiring is long enough to allow for dismantling and inspection. | 2 | |
| 28. | Wiring is wrapped neatly. | 2 | |
| 29. | A power switch is included and fitted to the enclosure. | 2 | |
| 30. | Wiring entering/exiting the enclosure is provided with a grommet/applicable fittings/sockets where applicable. | 2 | |
| 31. | A fuse/Protection is included and fitted correctly where applicable. | 2 | |
| 32. | Batteries/Transformer is mounted using a battery housing/mounting bracket and battery clip (NO double-sided tape). | 2 | |
| 33. | The project has a pilot light/LED installed in the enclosure showing when the circuit is operational. LED is mounted with a grommet or applicable fitting. (Switch is on – must go out when fuse is blown.) | 2 | |
| 34. | The project is fully operational and commissioned/installed in the enclosure. | 10 | |
| | Circuit Board Manufacturing Subtotal: | 65 | |
| | | | |
| | Circuit Diagram Subtotal: | 20 | |
| | Component List Subtotal: | 5 | |
| | Description of Operation Subtotal: | 25 | |
| | Tools/Instrument List Subtotal: | 5 | |
| | Circuit Board Manufacturing Subtotal: | 65 | |

| |
|---|
| TOTAL (PART 1 = 120 marks) |
|---|

| |
|--|
| NOTE: In projects where facets are not applicable, the projects should be marked and the totals adjusted accordingly. |
|--|

5.3 Design and make: Part 2**5.3.1 Enclosure design**

- Design an enclosure for your project.
- NO FREEHAND DRAWINGS.
- Draw using EGD equipment **OR** use a CAD program.
- Draw in first-angle orthographic projection.
- Add your drawings after this page.
- Use colour to enhance your drawing.

5.3.2 Manufacture the enclosure neatly according to your design. You may use pre-cut panels from metal, wood and/or Perspex/Plexiglass. You must, however, construct/assemble these parts. Injection moulded enclosures are also acceptable. It is important that your enclosure and the placement of the parts align with your design.

5.3.3 Choose a name for your device.
Write down the name of the device below.

5.3.4 Design a unique logo for your device, as well as a specification plate and attach it after this page.

[30]

5.4 Assessment of the design-and-make phase: Part 2

| NO. | FACET DESCRIPTION | Mark | Achieved = 1 Not achieved = * |
|--|---|-----------|----------------------------------|
| Enclosure Design | | | |
| 1. | Enclosure design is included in first-angle orthographic projection. | 2 | |
| 2. | Drawn design includes a title box and page border. | 1 | |
| 3. | Isometric drawing included additionally. | 2 | |
| 4. | Dimensions are included. | 2 | |
| 5. | The name of the device is written in the PAT document. | 1 | |
| 6. | The logo design and specification plate design is in the PAT document. | 2 | |
| Enclosure Design Subtotal: | | 10 | |
| Enclosure Manufacturing | | | |
| 7. | Enclosure matches the design. – Dimensions and placement correlate. | 1 | |
| 8. | Name of the device is attached on the enclosure. | 1 | |
| 9. | The logo design is attached on the enclosure. | 2 | |
| 10. | The logo design on the enclosure is durable and not merely a paper pasted on the enclosure (painted/used decoupage/screen printed/sublimation printed). | 2 | |
| 11. | The enclosure is manufactured from scratch/pre-cut parts. Does NOT include: cardboard, paper, margarine container Does include: sheet metal, Perspex, Plexiglas, wood, glass and other raw materials, injection-moulded plastic boxes | 5 | |
| 12. | Holes/Cut-outs in the enclosure are made with the appropriate tools. | 3 | |
| 13. | Specification plate with the learner's name, operating voltage, fuse rating and additional information on the project. | 2 | |
| 14. | Enclosure is neatly prepared, painted and aesthetically pleasing. | 2 | |
| 15. | The circuit board is mounted using appropriate methods inside the enclosure. (NO double-sided tape, Prestik, glue, chewing gum, masking tape, etc.) | 2 | |
| Enclosure Manufacturing Subtotal: | | 20 | |

| |
|--|
| TOTAL (PART 2 = 30 marks) |
|--|

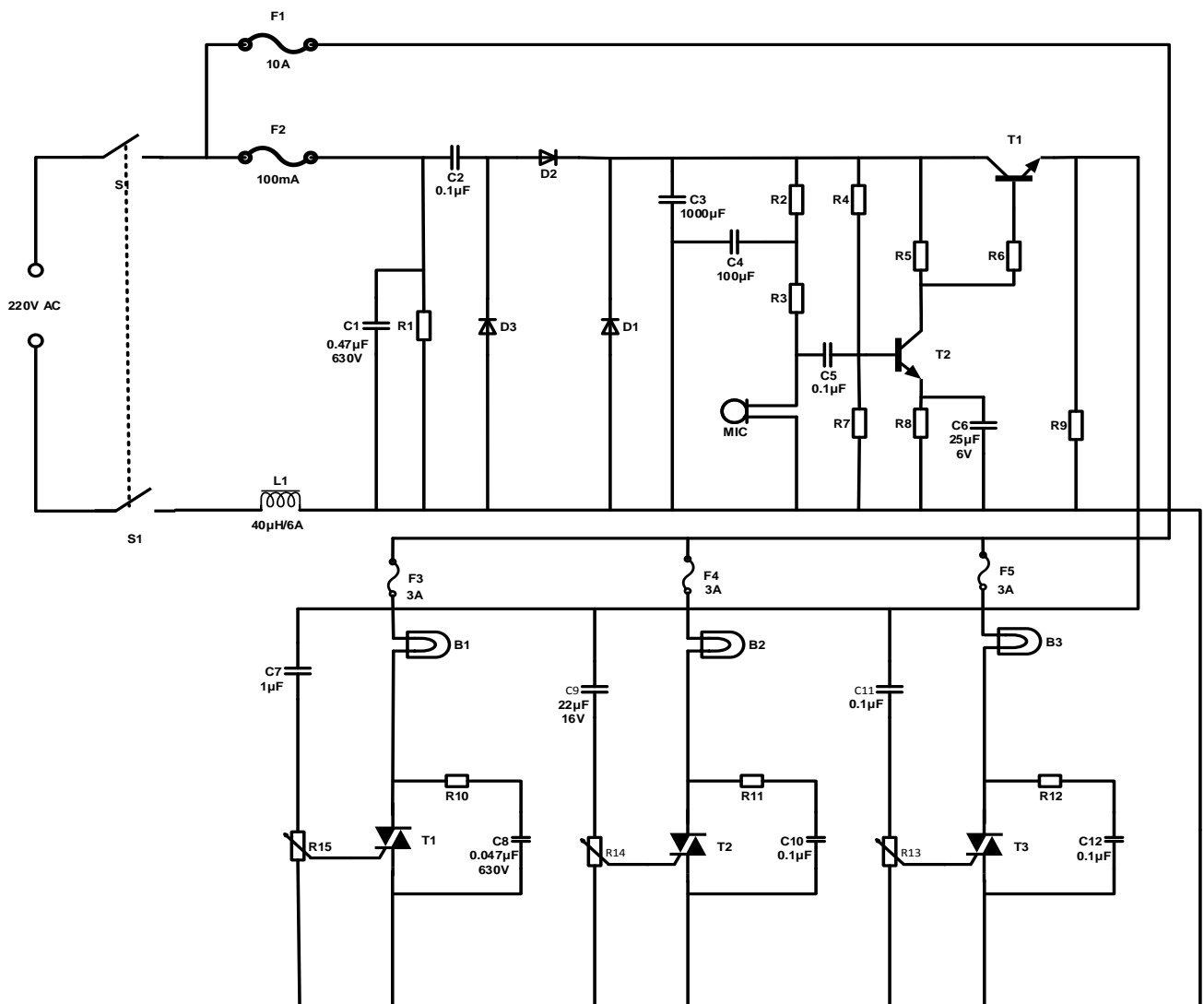
6. PROJECTS

6.1 Practical Project: Sound-to-light controller

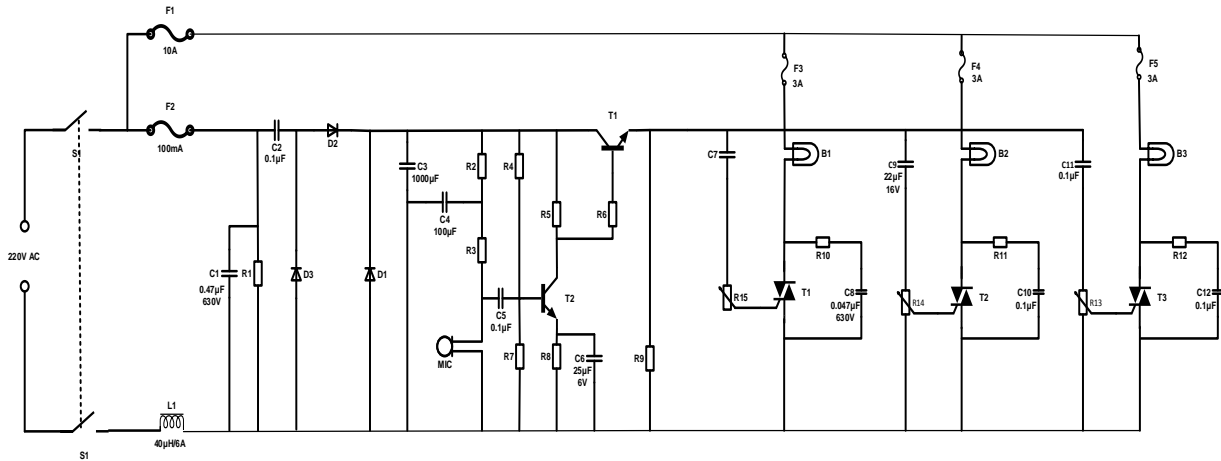
This sound-controlled lights circuit design is used to control the brightness of the lights attached to it in sync with the sound that is being captured by its microphone. This electronic circuit design is very common in discos, bars, at parties.

Usually sound-controlled lights are just connected in parallel with the loudspeakers. This configuration has two disadvantages: a very powerful amplifier can destroy the lights or, even worse, a defective light can destroy the amp. This problem is avoided by the circuit by not being connected directly to the amp. Instead, it picks up the sound with its microphone.

The power supply part is on the left of the electret microphone amplifier and the light controller part is on the right. The capacitors C2 and C3 are the capacitive voltage dividers and reduce the power supply level. Diodes D1 and D2 rectify the positive swing of the AC voltage. The network, composed of L1 and C1, protects the power line from voltages surges. In this circuit design, an electret microphone is used. Take note that there are two types of electret mics. The first type has three pins for power, ground, and output. The second type has only two pins. The second type is used for this circuit.



SOUND-TO-LIGHT CONTROLLER



1µF

ALTERNATIVE CIRCUIT

| COMPONENT LIST | |
|------------------------|-------------------------------------|
| R1 = 560 kΩ/1 W | C8, C12 = 0,047 µF/630 V |
| R2, R3 = 15 kΩ ¼ W | C9 = 22 µF 16 V |
| R4 = 33 kΩ ¼ W | C11 = 47 µF 16 V |
| R5, R6, R9 = 1 kΩ ¼ W | D1, D2 = 1N4004 |
| R7 = 18 kΩ ¼ W | D3 = 1N4742 12v/1 W |
| R8 = 560 Ω ¼ W | F1 10 A fuse 220 V |
| R10, R11, R12 = 100 kΩ | F2 100 mA fuse 220 V |
| P1, P2, P3 = 5 kΩ Pot | F3, F4, F5 220 V 3 A fuse |
| C1 = 0,47 µF 630 V | L1 = 40 µH 6 A |
| C2, C5 = 0,1 µF/220 V | B1, B2, B3 = 60 W incandescent lamp |
| C3 = 1 000 µF/16 V | Mic = low-impedance microphone |
| C4 = 100 µF/16 V | |
| C6 = 25 µF/6 V | |
| C7 = 1 µF 16 V | |

WARNING: Some parts in the circuit board are subject to lethal potential because the device is connected to 230 V AC. When plugging in the project, place it in a plastic or wooden box to prevent the circuit from shocking you. Avoid connecting this circuit to other appliances (e.g. to the output of an amplifier by means of a cable) because of the absence of a mains transformer. Use only the microphone in the main case to pick up the sound.

Practical Project 6.2: (Electronics): Dual voltage power supply

This project uses a centre-tapped transformer. The recommended rating of the transformer is 240 V to 18-0-18 V.

NOTE: Sometimes the transformer you purchase outputs more than the specified value, so be careful while choosing the transformer.

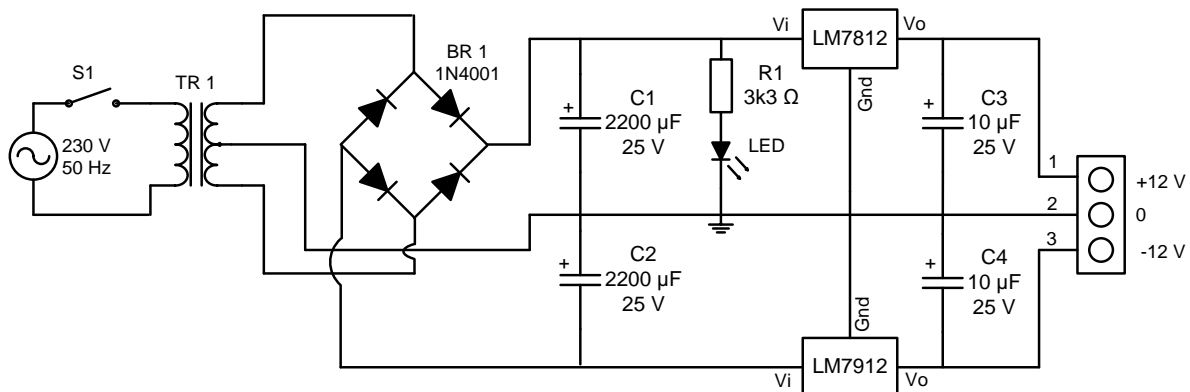
Capacitors C1 and C2 act as the smoothing capacitor; this is to even out any fluctuation in voltage. You can also add a bypass capacitor after the C1 and C2 to remove any AC noise which is not shown in the circuit. Besides the two voltage regulators, the 7812 gives positive 12 V and the 7912 gives you negative 12 V. Other variants of voltage regulator ICs can also be used.

NOTE: 78xx gives the positive output and 79xx gives the negative output.

Capacitors C3 and C4 are used as the bypass capacitor to remove the AC noise and give a pure and cleaner DC Signal.

Required resources:

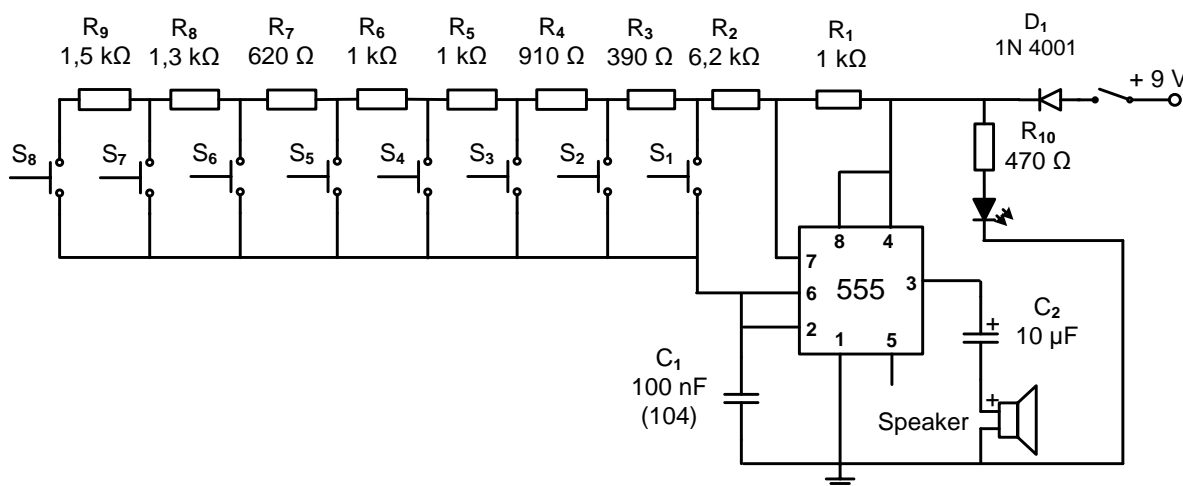
| TOOLS | MATERIALS | |
|-----------------------------|-------------------------------------|-------------------------------|
| Multimeter | 1 x transformer 240 to 15-0-15 volt | 1 x 7812 voltage regulator IC |
| Side cutters | - 4 x 1N4001 | 1 x 7912 voltage regulator IC |
| Wire strippers | 2 x 2 200 uF/25 v | 1x toggle switch |
| Soldering iron | 2 x 10 uF/25 v | 1 x in-line fuse and holder |
| Helping hands | 1 x 3,3 kΩ | 1 m mains supply cable |
| PCB etching tank or similar | 1 x red LED | 1 x 3 pin plug |
| Solder sucker | 2 x heat sink | 1 x PCB |
| | 2 x 3 pin terminal block | |

Circuit diagram:

Practical Project 6.3: Electronic piano

The electronic piano uses an astable mode of a common 555 timer integrated circuit to produce a tone that drives the speaker (piezo buzzer).

Each musical note has a specific frequency. The frequency produced by the 555 timer in astable mode relies on the values of capacitor (C_1) and two resistances (R_1 and a combination of R_2 to R_9). The resistance of R_2 to R_9 will vary depending on which push button is pressed.



| TOOL | MATERIALS | |
|-----------------------------|------------------------------|----------------------------------|
| Multimeter | 9 V battery and battery clip | 470 Ω resistor |
| Side cutters | SPST switch | LED red x 1 |
| Long-nose plier | Fuse and fuse holder | 100 nF ceramic capacitor (104) |
| Wire strippers | 1N 4001 diode | 10 μF electrolytic capacitor 16V |
| Soldering iron | 1 kΩ resistor x 3 | IC NE555 |
| Solder sucker | 390 Ω resistor | Speaker 8 Ω/buzzer |
| Helping hands | 910 Ω resistor | PCB |
| PCB etching tank or similar | 620 Ω resistor | Solder |
| | 1k3 Ω resistor | Etching chemicals |
| | 1k5 Ω resistor | |

NOTE:

All circuits MUST include an ON/OFF switch with a ON indicator and fuse protection.

7. CONCLUSION

On completion of the practical assessment task learners should be able to demonstrate their understanding of the industry, enhance their knowledge, skills, values and reasoning abilities as well as establish connections to life outside the classroom and address real-world challenges. The PAT furthermore develops learners' life skills and provides opportunities for learners to engage in their own learning.