basic education

Department:
Basic Education
REPUBLIC OF SOUTH AFRICA

NATIONAL SENIOR CERTIFICATE

GRADE 12

ELECTRICAL TECHNOLOGY: DIGITAL ELECTRONICS

NOVEMBER 2022

MARKING GUIDELINES

MARKS: 200

These marking guidelines consist of 16 pages.

INSTRUCTIONS TO THE MARKERS

1. All questions with multiple answers imply that any relevant, acceptable answer should be considered.

2. Calculations:

   2.1 All calculations must show the formulae.

   2.2 Substitution of values must be done correctly.

   2.3 All answers MUST contain the correct unit to be considered.

   2.4 Alternative methods must be considered, provided that the correct answer is obtained.

   2.5 Where an incorrect answer could be carried over to the next step, the first answer will be deemed incorrect. However, should the incorrect answer be carried over correctly, the marker has to re-calculate the values, using the incorrect answer from the first calculation. If correctly used, the candidate should receive the full marks for subsequent calculations.

3. These marking guidelines are only a guide with model answers. Alternative interpretations must be considered and marked on merit. However, this principle should be applied consistently throughout the marking session at ALL marking centres.

QUESTION 1: MULTIPLE-CHOICE QUESTIONS

1.1 C ✓ (1)

1.2 A ✓ (1)

1.3 C ✓ (1)

1.4 D ✓ (1)

1.5 C ✓ (1)

1.6 D ✓ (1)

1.7 C ✓ (1)

1.8 D ✓ (1)

1.9 D ✓ (1)

1.10 A ✓ (1)

1.11 B ✓ (1)

1.12 D ✓ (1)

1.13 A ✓ (1)

1.14 C ✓ (1)

1.15 B ✓ (1)

[15]

QUESTION 2: OCCUPATIONAL HEALTH AND SAFETY

2.1 The employer should be respected ✓
The employer should not be discriminated against. ✓
Your right to fair labour practices.
Your right to work reasonable hours.
Your right to belong to a trade union.
Your right to earn a living wage.
Your right not to be discriminated against. (2)

2.2 Move in an orderly manner. ✓
Follow the evacuation route as displayed in your workshop. ✓
Move to the designated assembly point in a calm and orderly manner. (2)

2.3 Misusing equipment is a dangerous practice which might damage the equipment ✓ and render it unsafe, compromising the safety and or threatens the health of others. ✓ (2)

2.4 An employer shall not dismiss an employee ✓ without the correct procedures being followed.
An employer shall not reduce the remuneration of an employee as punishment.
Alter terms of condition of employment to one that is less favourable. ✓
Alter a position relative to other employees employed by that employer to disadvantage them. (2)

2.5 Quantitative risk analysis✓
Qualitative risk analysis✓ (2)
[10]

QUESTION 3: SWITCHING CIRCUITS

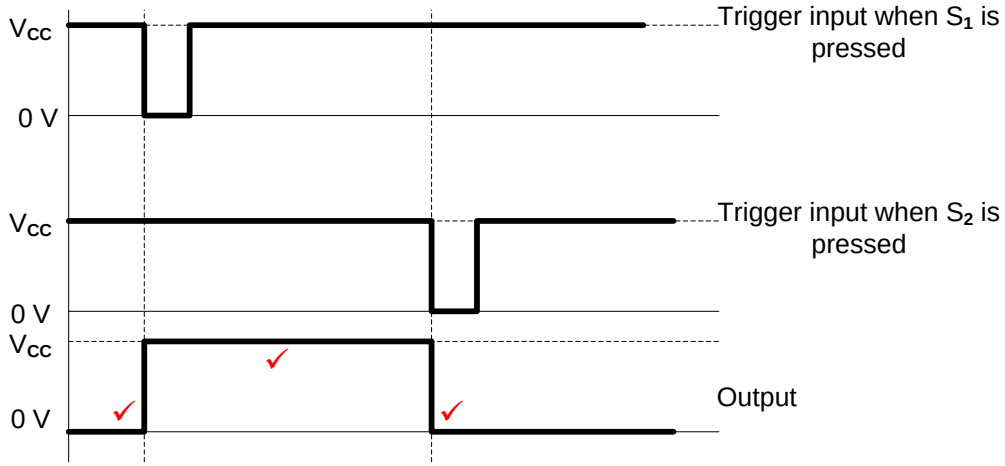
3.1 The output of a monostable multivibrator has only one stable state. ✓
The output of an astable multivibrator will toggle between high and low states continuously. ✓
The output of an astable multivibrator has no stable state. (2)

3.2 3.2.1 The bistable multivibrator is used in automated applications. ✓
(where a device is required to run continuously back and forth on the same path)
Counting circuits.
Storing circuits.
Frequency divider circuits.
Latches. (1)

3.2.2 To prevent the IC from resetting. ✓ When a positive pulse (trigger pulse 1) is applied to the Trigger input, the output will change to low (0 V) ✓ and remain there until a low pulse (trigger pulse 2) is applied. ✓ (3)

3.2.3 Without pull-up resistor R_2 connected to the supply, the voltage on pin 2 will continuously vary ✓ between $\frac{1}{3}V_{CC}$ and 0 V.✓(floating) (2)

3.2.4



NOTE:

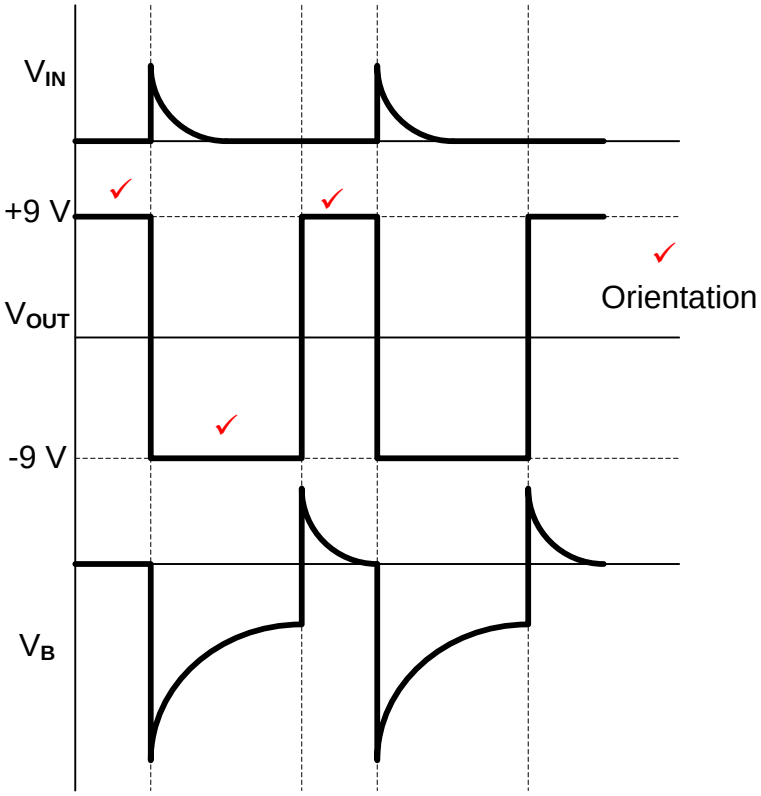
An inverted output waveform the candidate will lose 1 mark for orientation and be awarded 2 marks for the correct trigger points. (3)

3.3 3.3.1 C_2 and R_3 sets the time period ✓ that the circuit will remain in its changed state. ✓ (2)

3.3.2 0 V ✓ (1)

3.3.3 The moment a positive pulse is applied to the inverting input, the output changes from positive saturation (9 V) ✓ to negative saturation (-9 V) ✓ for the duration of the RC time constant. ✓ (3)

3.3.4



NOTE:
An exact inverted output waveform will lose 1 mark for orientation and be awarded 3 marks. (4)

3.4 3.4.1 Positive ✓ (1)

3.4.2 The output changes from +9 V to –9 V the moment V_A (inverting voltage) becomes higher than V_B. (non-inverting voltage) ✓ (1)

3.4.3 An increase in the value of R_F will increase the RC time constant ✓ on the input of the op amp, because the capacitor takes longer to charge up to the voltage V_B, ✓ it results in a decrease in frequency on the output. ✓ (3)

3.5 3.5.1 +9 V and -9 V ✓ (1)

3.5.2 R_F and R_1 used to determine the trigger voltage level ✓ on the non-inverting input. ✓
If a candidates mention that R_F and R_1 is a voltage divider 1 mark is allocated. (2)

3.5.3 The output changes from high to low when the input voltage (V_{in}) is higher ✓ than the upper trigger voltage (V_X). ✓ (2)

3.6
- The op amp compares the voltages appearing on its two input terminals. ✓
- When the input voltage on the inverting input is lower than the reference voltage ✓
- the op amp is driven to positive saturation. ✓
- As soon as the input on the inverting terminal is higher than the reference voltage,
- the op amp is driven into negative saturation. (3)

3.7 3.7.1 Inverting summing amplifier. ✓ (1)

3.7.2 The gain of the amplifier is -1, ✓ because $R_1=R_2=R_3=R_F$ ✓ (2)

3.7.3 $V_{OUT} = -(V_1 + V_2 + V_3)$ ✓

$= -(0{,}9 + 1{,}2 + 2{,}1)$ ✓

$= -4{,}2\ V$ ✓ (3)

$$V_{OUT} = -\left(V_1 \times \frac{R_F}{R_1} + V_2 \times \frac{R_F}{R_2} + V_3 \times \frac{R_F}{R_3}\right)$$

$$= -\left(0{,}9 \times \frac{22 \times 10^3}{22 \times 10^3} + 1{,}2 \times \frac{22 \times 10^3}{22 \times 10^3} + 2{,}1 \times \frac{22 \times 10^3}{22 \times 10^3}\right)$$

$$= -4{,}2\ V$$

3.7.4 An increase in the value of the feedback resistor will decrease negative feedback ✓ resulting in an increase in the gain. ✓
Gain will increase, therefore output voltage will also increase. (2)

3.8 3.8.1 How long the input voltage has been present. ✓
The value of the input voltage. ✓
The frequency
Value of the resistor and capacitor
The RC-time constant
The value of the supply voltage (2)

3.8.2 Both inputs to the op amp are kept at 0 V ✓ according to Ohm's law when a constant positive voltage is applied across the input resistor it causes a constant fixed current to flow, ✓ which is fed via the virtual ground point to the capacitor, ✓ this means that the voltage on its right-hand plate will decrease at a fixed linear rate towards -V. ✓ (4)

3.8.3 When the RC time constant is long, the capacitor will charge slowly ✓ causing the slope of the output to decrease. ✓ The output will change direction before reaching saturation. (2)
[50]

QUESTION 4: SEMICONDUCTOR DEVICES

4.1 4.1.1 0 V ✓
If a learner refers to '*virtual ground*' it will be accepted. (1)

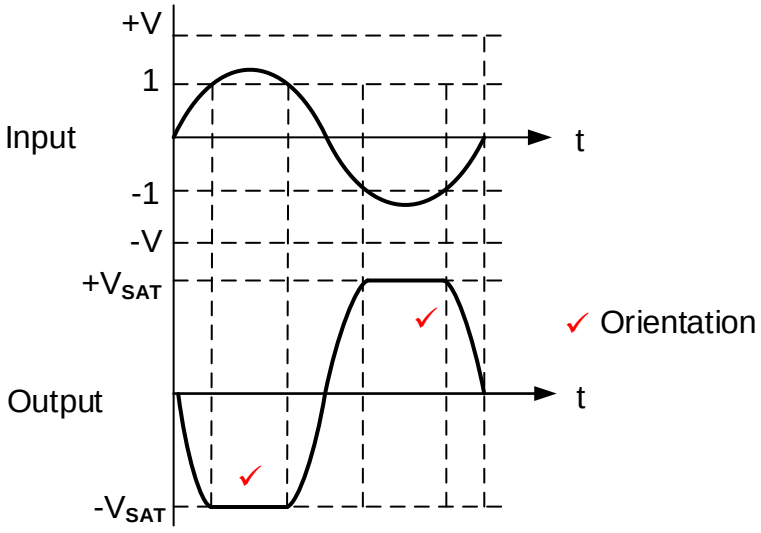
4.1.2
$$A_V = -\frac{R_F}{R_{IN}} \quad ✓$$
$$= -\frac{1400}{1000} \quad ✓$$
$$= -1{,}4 \quad ✓$$
(3)

4.1.3 The output signal will have a 180º phase shift. ✓
The output signal will be inverted. (1)

4.2 4.2.1 Along DA ✓and BE✓ of the graph FIGURE B (2)

4.2.2
$$A_V = \frac{V_{OUT}}{V_{IN}} = \frac{AC}{OC} \quad ✓$$
$$= \frac{+13}{-1} \quad ✓$$
$$= -13 \quad ✓$$
(3)

4.2.3



(3)

4.2.4 The gain of the amplifier will increase. ✓
Output voltage will be increased. ✓ (2)

4.3 4.3.1 Pin 7 provides the discharge path for the timing capacitor and timing resistor. ✓
Pin 7 provides a discharge path to ground. (1)

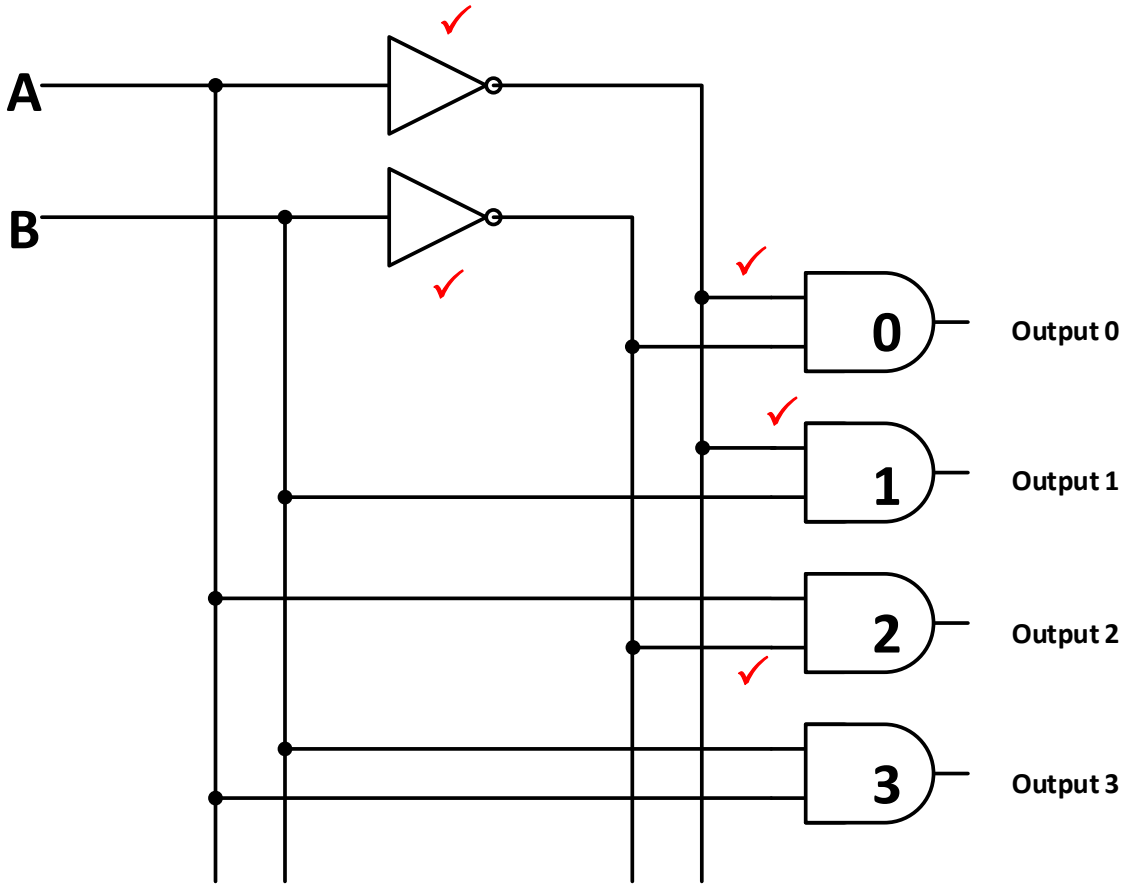
4.3.2 When the voltage at Pin 2 falls below 1/3 ✓ of the supply voltage, ✓ it pulls Pin 2 to ground ✓, the output goes high, ✓ thereby activating the 555 circuit. (4)
[20]

QUESTION 5: DIGITAL AND SEQUENTIAL DEVICES

5.1 5.1.1 A = any acceptable value between the range of 3 V to 18 V ✓
Supply voltage will be accepted
B = Clock Input ✓ (2)

5.1.2 The main purpose of the driver is to provide the necessary current ✓ to activate the seven-segment display. ✓
A seven-segment display driver is used to convert a four-bit binary code to a seven-segment binary code to that the seven-segment display can show a decimal number for the user. (2)

5.2



(5)

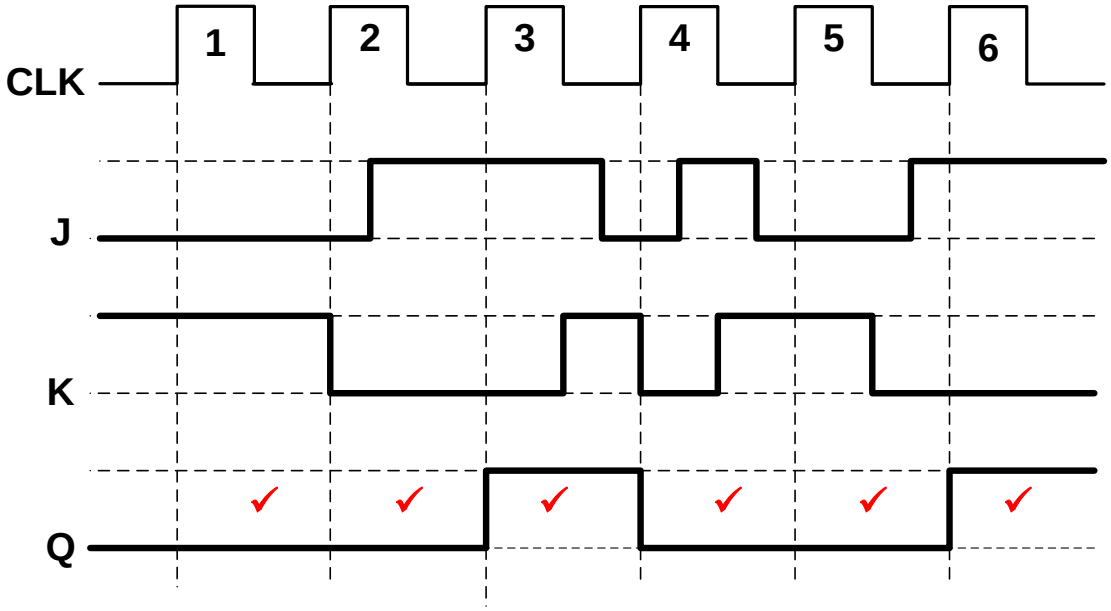
5.3 5.3.1 X = XOR ✓
Y = AND ✓ (2)

5.3.2

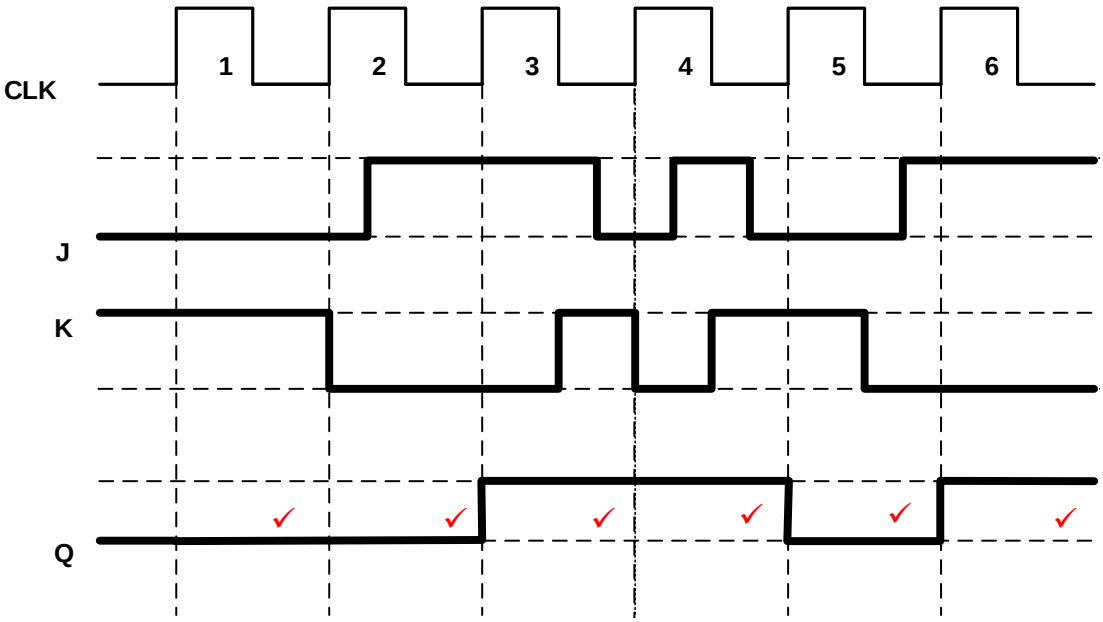
A	B	Σ	c_{out}
0	0	0	0
0	1	1✓	0✓
1	0	1✓	0✓
1	1	0✓	1✓

(6)

5.4



OR



(6)

5.5 5.5.1 Active Low Latch ✓($\bar{S}\bar{R}$ latch) (1)

5.5.2

INPUTS		OUTPUTS	
$\overline{S}$	$\overline{R}$	Q	$\overline{Q}$
0	0	Unpredictable ✓✓	
0	1	1	0✓
1	0	0✓	1✓
1	1	No change✓	

INPUTS		OUTPUTS	
$\overline{S}$	$\overline{R}$	Q	$\overline{Q}$
0	0	1✓	1✓
0	1	1	0✓
1	0	0✓	1✓
1	1	No change✓	

NOTE: The first table is correct, but the second table will also be accepted as it is from the textbook. (6)

5.6 5.6.1 Up-counter is simply a digital counter that counts up ✓ to some predefined increment. ✓ (2)

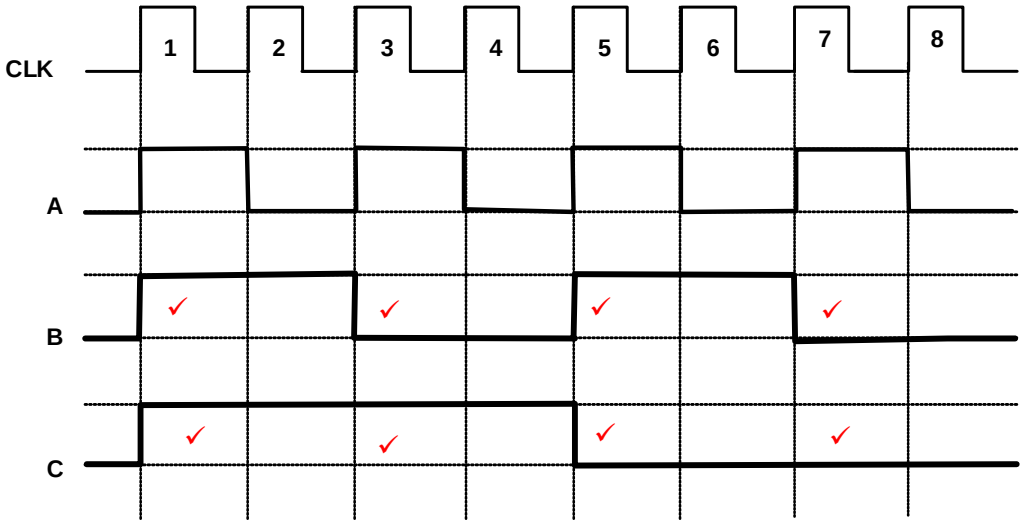
5.6.2 Up/down is a counter that can change state in either direction, ✓under the control of an up/down selector input. ✓ (2)

5.6.3 A ripple counter is a type of asynchronous counter in which the clock pulse ripples✓ through the circuit. ✓

OR

Ripple counter consists of a series connection of complementing flip-flops and the output of each flip-flop is connected to the clock input of the next higher-order flip-flop. (2)

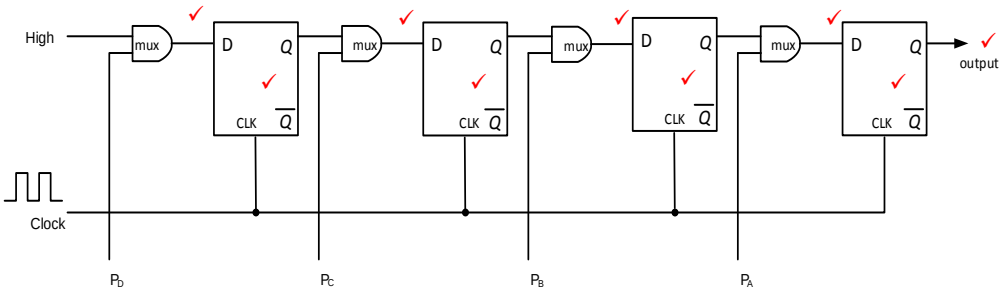
5.7 5.7.1



(8)

5.7.2 The Down counter has fewer logic gates ✓ than the Up/Down counter thereby reducing propagation delay ✓ causing it to operate faster. (2)

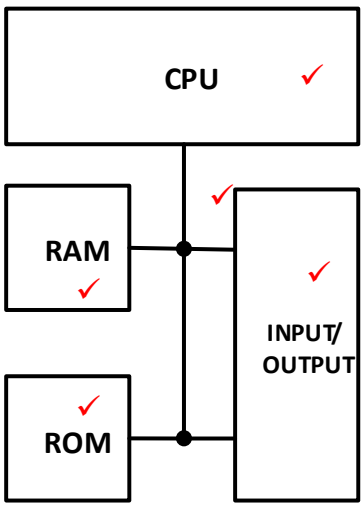
5.8



(9)
[55]

QUESTION 6: MICROCONTROLLERS

6.1



NOTE: 1 mark for each correctly labelled block (x 4)
1 mark for all connecting lines (1)
If the learners showed all the components but incorrectly placed (2) (5)

6.2 It fetches each instruction ✓ that needs to be executed in a program ✓ by issuing control signals to the hardware. ✓
It then decodes the instruction ✓ and finally issues more control signals to the hardware to actually execute it. ✓ (5)

6.3 6.3.1 The TRIS register sets the 'direction' of the input ✓ and output pins ✓ by setting some bits of the TRIS register to either '0' or '1'. (2)

6.3.2 By setting the TRIS register bits low '0' configures the pins as 'output' pins ✓ and setting the register bits to high '1' configures the same pins to 'input' pins. ✓ (2)

6.4 The majority of input signals from inputs are of an analogue nature ✓ whereas the microcontroller operates purely in digital. ✓ Therefore A/D converters are needed to convert the analogue input signals to digital. ✓ (3)

6.5 6.5.1 A = Transmitter/Sender ✓
B = Receiver ✓
C = Request ✓ (3)

6.5.2
- Data is sent in a pre-arranged pattern of bits called bytes. ✓
- There is no timing signal or clock pulse required. ✓
- The flow of data from the sender to the receiver is monitored/ checked by the parity bits, namely the 'start bit', usually binary '0', and the 'stop bit' which are added at the beginning and at the end of each byte. ✓
- Data moves one byte at a time ✓
- When a sender receives data, it sends a request to the receiver and waits for an acknowledge signal ✓
- Once the signal is received, the sender then sends the data together with the start and stop parity bits ✓ (6)

OR

- Data is sent in a pre-arranged pattern of bits.
- Once both ends of the system (sender and receiver) have agreed on the pattern then communication can take place, with no timing signal or clock pulse required.
- 'Parity' bits are added to the front and end of each binary byte or small group of bits.
- A parity bit is simply an additional bit added to a block of binary bits to keep a check on their order.
- Bits are grouped together consisting of both data and control bits. If the signal is not synchronised the receiver will not be able to distinguish when the next group of bits will arrive.
- To overcome this the data is preceded by a 'start bit', usually binary '0', the byte is then sent and a 'stop bit' which is added to the end.
- Each byte to be sent now incorporates extra control data. In addition to the control data, small gaps are inserted between each 'chunk' to distinguish each group.

6.5.3 It does not need a synchronising clock pulse between sender and receiver. ✓
It is a 'peer-to-peer' system where data can be transferred in both directions between the two devices. ✓ (2)

6.6 6.6.1 Serial Peripheral Interface. ✓ (1)

6.6.2 Full duplex mode. ✓ (1)

6.6.3
- The SPI communicates in full duplex mode.
- Communication is initiated by the master, generating the clock signal through SCK to the port pin of the slave
- The master switches the SS pin to a low voltage state which activates the slave ✓
- The master sends the data one bit at a time to the slave along the MOSI line. The slave reads the bits as they are received ✓
- If a response is needed, the slave returns data one bit at a time to the master along the MISO line ✓
- The master reads the bits as they are received ✓ (4)

OR

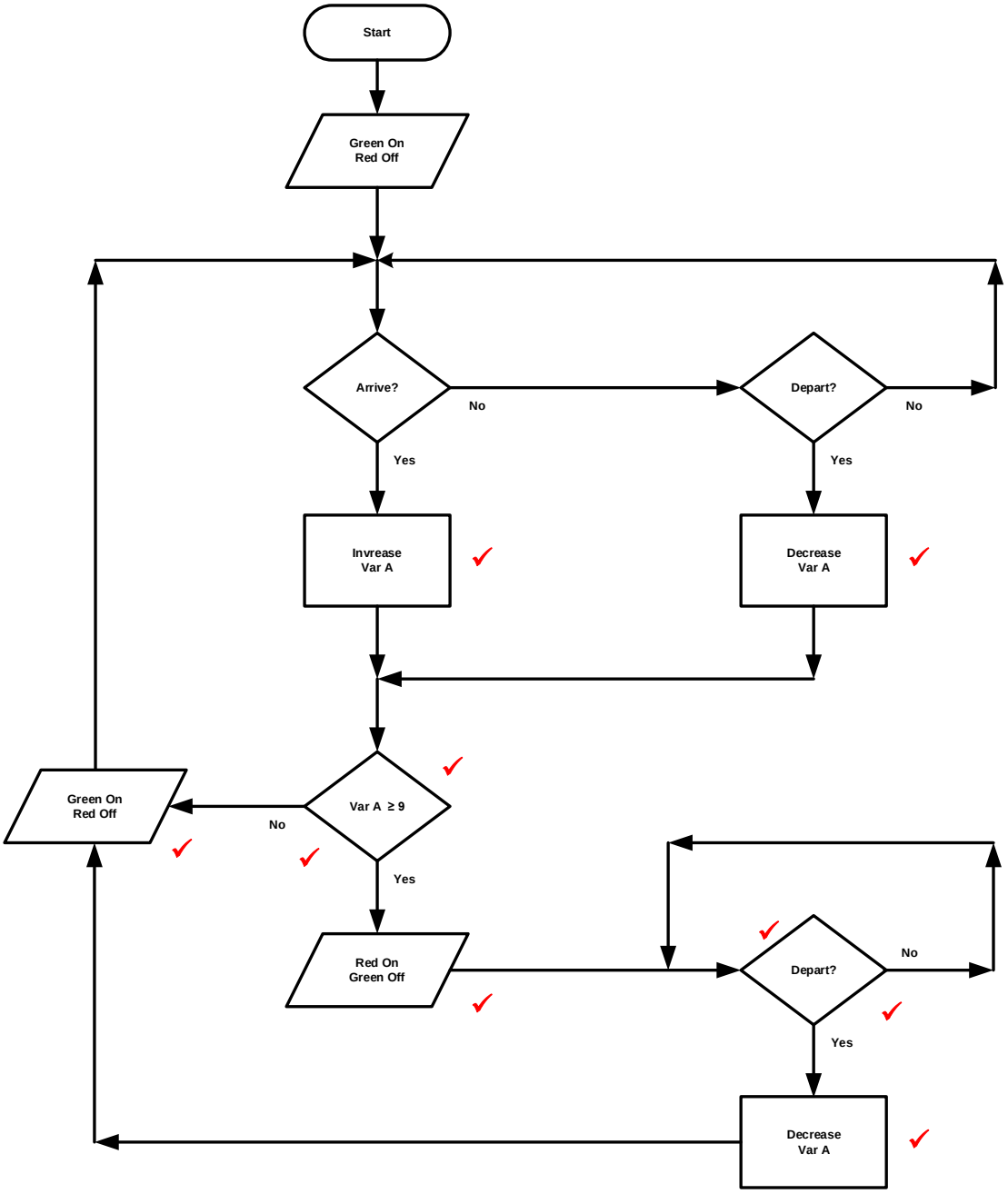
- A serial connection using only one line is asynchronous because there is no additional clock line to synchronise exactly when data is sent or that both sides are running at the same speed. As computers rely on everything to be synchronised, this can present problems when two systems with different clocks try to communicate.
- To get around this, asynchronous serial connections add extra start and stop bits to help the receiver synchronise the data as it arrives.
- By adding an additional synchronising clock line this can hold both sides perfectly synchronised, called CLK or SCK.
- The side generating the clock is called the master and the other side is called the slave.
- The master sends data to the slave on the data line and if the slave needs to send a signal in response back the master first sends a number of clock pulses which are pre-arranged, and then the slave sends the data on a third line called MISO.

6.6.4 SPI supports higher speed full-duplex communication ✓
SPI draws little power ✓
SPI can operate at extremely high speeds (2)

6.7 6.7.1 Looping is when a task is repeated ✓ over and over until the condition is true. ✓ (2)

6.7.2 A conditional statement is a mechanism that allows for conditional execution of instructions ✓ based upon the outcome of a conditional statement, ✓ which can either be true or false. ✓ (3)

6.8



NOTE: 1 mark for each correctly labelled symbol (x 7)
1 mark for each correct placement of Yes/No (2)

(9)
[50]

TOTAL: 200